NASA CR-132486

A FOLLOW-ON STUDY FOR

MINIATURE SOLID-STATE PRESSURE TRANSDUCER

Prepared for

National Aeronautics and Space Administration
Langley Research Center
Langley Station
Hampton, Virginia

Final Report

August 1974

(Prepared under Contract NASI-9005 by the Engineering and Environmental Sciences Division of the Research Triangle Institute, Research Triangle Park, North Carolina.)

FOREWORD

This report was prepared by the Research Triangle Institute, Research Triangle Park, North Carolina on NASA Contract NAS1-9005, "A Follow On Study for Miniature Solid State Pressure Transducers." This investigation was performed by members of the Envrionmental and Engineering Programs Group of the Research Triangle Institute. Staff members contributing significantly to this investigation include Dr. Robert M. Burger, Dr. J. J. Wortman, C. D. Parker, R. P. Donovan, A. D. Brooks, H. L. Honbarrier and R. T. Pickett. This work was administered under the direction of the Flight Instrument Division, Langley Research Center, by Mr. Charles A. Hardesty.

The work was carried out in two parts chronologically. Part A describes the first investigation, a totally Research Triangle Institute in-house effort. The time period for this work was March 1969 to August 1970. The activities described in Part B include the liberal use of outside vendors to supply various parts and services in the manufacture of prototype test units. The period of performance for this portion of the contract was December 1970 to June 1974. The RTI Project Leader for Part A of this effort was C. D. Parker and for Part B was R. P. Donovan.

ABSTRACT

This two part final report summarizes the activities of a developmental program to design, fabricate and test an absolute pressure transducer based upon the piezojunction properties of silicon. The prime problem addressed here is the development of a housing capable of applying the high stress levels needed for sensitive piezojunction operation but at the same time, free from the creep effects and the fragility that limit the usefulness of previous designs.

The first part of the report describes the initial fabrication and tests and reviews the theory of sensor performance. The second part incorporates two recommendations of the first part (the use of commerically manufactured silicon planar mesa diodes and the adoption of an all-silicon structure for loading) and presents some preliminary test data on the transducers thus fabricated. These initial measurements show much improved performance over any previously fabricated piezojunction transducers but testing is incomplete and several problems in manufacturing technology remain.

CONTENTS
PART A: March 1969 - August 1970

CONTENTS
PART B: December 1970 - June 1974

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (continued)

LIST OF ILLUSTRATIONS (continued)

LIST OF SYMBOLS

a, b, c	constants
D_d	deformation potential coefficient (eV)
D_u	deformation potential coefficient (eV)
D_u'	deformation potential coefficient (eV)
E_o	energy corresponding to zero strain (eV)
E_F	energy of the Fermi level (eV)
E_{V1}	energy of the j = 3/2, "heavy" hole band (eV)
E_{V2}	energy of the j = 3/2, "light" hole band (eV)
E_{V3}	energy of the j = 1/2 split-off hole band (eV)
E_{Ci}	energy of the conduction band minima (eV)
e	hydrostatic strain
e_i	strain components referred to crystal axes
Γ_{25}'	valence band edge point
$\gamma_\nu(e)$	ratio of minority carrier density with strain to that without strain
$\hbar$	Planck's constant ($6.624/25 \times 10^{-27}$ erg's)
I_T	total p-n junction current (A)
I_I	ideal p-n junction current (A)
I_R	generation-recombination junction current (A)
j	angular momentum quantum number
k	Boltzmann's constant (8.62×10^{-5} eV/°K)
$\bar{k}$	wave vector (cm^{-1})
m_{Ci}	effective electron masses associated with the conducting band energy minima (g)
m_{Vi}	effective hole masses associated with the valence band energy maxima (g)

LIST OF SYMBOLS (continued)

n	electron density (cm^{-3})
n_o	electron density corresponding to zero stress (cm^{-3})
p	hole density (cm^{-3})
p_o	hole density corresponding to zero stress (cm^{-3})
q	electronic charge (1.602×10^{-19} C)
σ	stress level ($dynes/cm^2$)
σ_b	base-region stress ($dynes/cm^2$)
σ_e	emitter-region stress ($dynes/cm^2$)
T	absolute temperature (°K)
V	p-n junction voltage (V)
V_B	unstressed breakdown voltage of a p-n junction (V)
Ξ_d	deformation potential coefficients
Ξ_u	deformation potential coefficients

A FOLLOW-ON STUDY FOR MINIATURE SOLID-STATE PRESSURE TRANSDUCERS

PART A: March 1969 - August 1970

SECTION I

INTRODUCTION

The work discussed in this report was a continued effort to exploit the stress-sensitive piezojunction effect in fabricating a solid-state pressure transducer. The piezojunction effect refers to the sensitivity of the electrical properties of a p-n junction to mechanical stress (or strain) in the vicinity of the junction. It occurs at high stress levels; e.g., beginning at 10^9 dynes/cm^2 in silicon, and is characterized by an exponential increase in minority carrier density as stress is increased above the threshold level. Consequently, the presence of such a stress is readily apparent in the V-I characteristics of a p-n junction.

This work was preceded by two years of effort; i.e., Contract Nos. NAS1-6249 and NAS1-7489, to demonstrate the feasibility of using the piezojunction effect as the sensory phenomenon in a pressure transducer. Several pressure transducers were fabricated, and these have been described (Refs. 1, 2). By way of review, the most successful transducers were fabricated using a silicon needle sensor in which the p-n junction was fabricated in the tip of a silicon needle. This unique configuration had several advantages including the elimination of alignment-related problems that are inherent in the indenter point configuration, the problem of coupling stress to such a minute region of a much larger silicon plane, and a stressed area to total junction area ratio approaching unity. The silicon needle sensor also has a serious handicap. Fabricating the needle sensor is extremely difficult. Numerous individual hand operations and operator judgment decisions are required and, consequently, laboratory yields were low. Although a technology evolved at RTI for fabricating the needle sensor, it was difficult to reproduce in the laboratory and was never tried on a production line basis. More recently, only configurations which are compatible with standard semiconductor processing practices and adaptable to a production line technique were considered. A second disadvantage of the needle sensor is fragility. The units fabricated into sensitive pressure transducers were frequently damaged by slight overpressures.

Pressure transducers fabricated more recently; i.e., during the current effort, are a significant improvement over earlier transducers. The sensitive element is a capsule diode; i.e., a planar-mesa diode structure sealed between two glass diaphragms. Although considerable

difficulty was encountered in the fabrication of the diode structure in our limited laboratory, the entire process requires only standard state-of-the-art processes and should present no significant problems to a production line facility. Additionally, the capsule diode structure is an absolute pressure gauge with a built-in vacuum reference and cannot be damaged by oven pressure. Unlike preceding configurations, the capsule diode is designed to see a minimum stress during storage conditions; i.e., one atmosphere pressure.

Capsule diode pressure transducers have been fabricated. These have been disappointing in terms of demonstrated sensitivity. Several factors have limited the achievement of the sensitivity potential of the piezojunction phenomenon. First, junction yields were very low and many of the transducers fabricated began with less than ideal junction sensors. Secondly, the semiconductor processing facility in use was not state-of-the-art and the ideal junction geometry could not be achieved. Finally, other parts; e.g., the glass wafers, were not standard items and were hand-fabricated in a facility not adapted for working with glass. However, transducers were fabricated that detected absolute pressure changes of approximately one mm Hg and these had a built-in vacuum reference and a dynamic range of one atmosphere. There is little doubt that a state-of-the-art semiconductor processing facility with a glass-oriented technology can fabricate a similar transducer that realizes the promised sensitivity.

SECTION II

THEORETICAL CONSIDERATIONS - A SUMMARY

A complete theoretical discussion of the piezojunction phenomenon has been published by Wortman, et al., (Refs. 3-5). It has been summarized in reports on previous feasibility studies, and an extended summary is included in this section in the interest of completeness.

Energy Band Considerations

The electrical characteristics of semiconductors and the piezojunction phenomenon are conveniently described in terms of the energy band structure. Silicon, as is the case for all semiconductors, has a forbidden energy region (energy gap) separating the valence energy levels (valence band) and the conduction energy levels (conduction band). In momentum space ($\bar{k}$-space), the maximum valence levels in silicon occur at $\bar{k}$ = (000) and the minimum conduction levels occur in the <100> directions. The maximum valence levels, Γ'_{25}, are degenerate in energy with a separation resulting from the two angular momentum quantum numbers, j = 3/2 and j = 1/2. The j = 1/2 level is approximately 0.04 eV below the j = 3/2 and is neglected in the computations that follow in this section. The Γ'_{25} level is also degenerate at k = (000) and is slightly split for k ≠ (000) due to spin orbit coupling. The Γ'_{25} valence levels of silicon near k = (000) are illustrated for silicon in Fig. 1. The splitting of the Γ'_{25} (j = 3/2) level for k ≠ (000) causes the effective masses for the two levels to be different, and the upper and lower levels are frequently referred to as "heavy" holes and "light" holes, respectively.

When stress is applied to the silicon crystal, the Γ'_{25} (j = 3/2) energy levels become non-degenerate as illustrated in Fig. 2. E_{V1} and E_{V2} are the Γ'_{25} (j = 3/2) "heavy" and "light" hole energy levels, and E_{V3} is the Γ'_{25} (j = 1/2) energy level. Since it is the width of the forbidden energy gap that is of interest, it is convenient to consider the change in the Γ'_{25} (j = 3/2) energy levels with strain. These are given by

$$\Delta E_{V1} = E_{V1} - E_o = D_d e + \{(\tfrac{2}{3} D_u)^2 (e_1^2 + e_2^2 + e_3^2 - e_1e_2 - e_1e_3 - e_2e_3) + \tfrac{1}{3} (D'_u)^2 (e_4^2 + e_5^2 + e_6^2)\}^{1/2}, \quad (1)$$

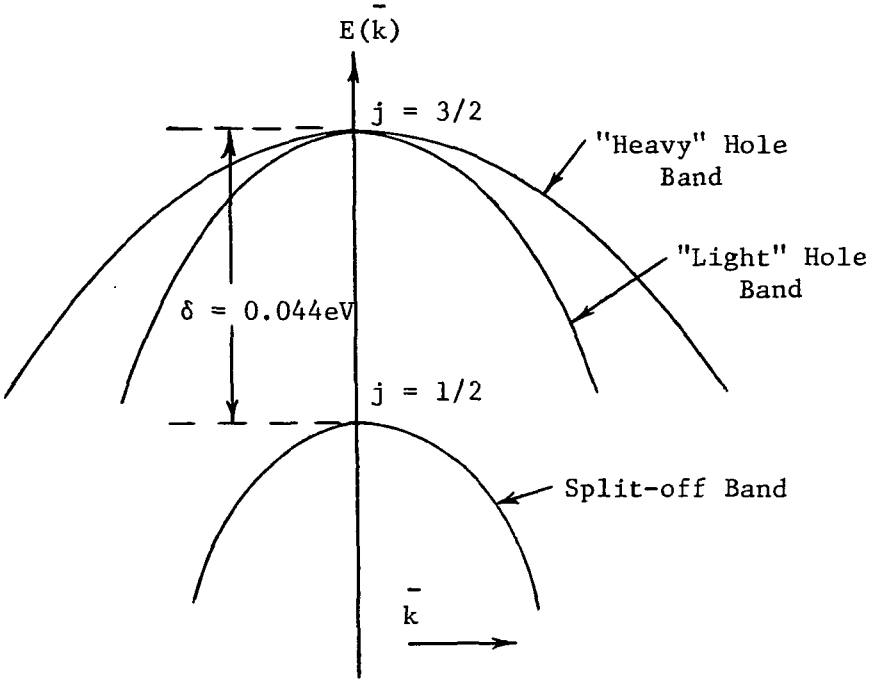


Figure 1. The Valence Bands of Silicon Near $\bar{k} = 0$ (Ref. 5)

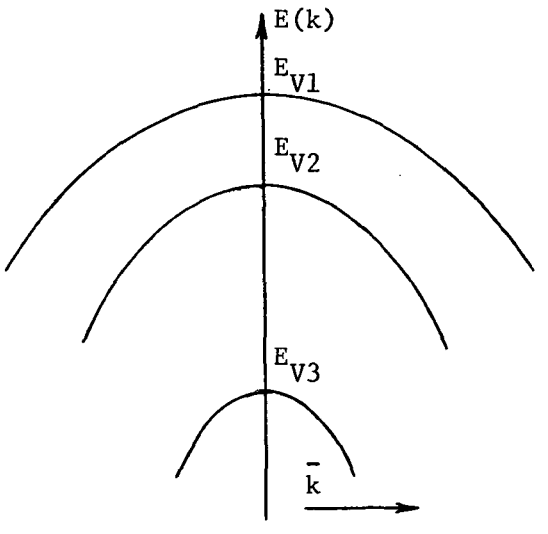


Figure 2. The Split Valence Bands of Silicon for a Compressional Stress (Ref. 5)

and

$$\Delta E_{V2} = E_{V2} - E_o = D_d e - \{(\frac{2}{3} D_u)^2 (e_1^2 + e_2^2 + e_3^2 - e_1 e_2 - e_1 e_3 - e_2 e_3) + \frac{1}{3} (D_u')^2 (e_4^2 + e_5^2 + e_6^2)\}^{1/2} , \quad (2)$$

where the D's are the deformation potential coefficients, and the e_i's are the components of strain (see Appendix C). More specifically, D_d is the energy level shift per unit dilation of the Γ_{25}' (j = 3/2) band edge, D_u is proportional to the splitting of the band edge induced by uniaxial shear strain along the [100] axis, and D_u' is proportional to the band edge splitting induced by uniaxial shear strain along the [111] axis. E_o is the unstrained Γ_{25}' (j = 3/2) energy level (Ref. 3).

Strain also induces changes in the conduction bands, and changes in the conduction band minima are of equal importance with changes in the valence band maximum. Silicon has six conduction band minima located along the principal crystal axes. Since these minima change in pairs; i.e., since one cannot distinguish between the conduction band minima located along the [100] and [$\bar{1}$00] axes, only three conduction band minima need be considered, E_{C1}, E_{C2} and E_{C3}. Changes in these conduction band minima in the stress region of interest are given by (Ref. 3)

$$\Delta E_{C1} = \Xi_d e + \Xi_u e_1 ,$$

$$\Delta E_{C2} = \Xi_d e + \Xi_u e_2 , \quad (3)$$

$$\Delta E_{C3} = \Xi_d e + \Xi_u e_3 ,$$

where the Ξ's are the deformation potential coefficients, and the e_i's are the engineering strain components along the crystal axes, (see Appendix C.) and

$$e = e_1 + e_2 + e_3 . \quad (4)$$

Changes in the valence band and conduction band maxima and minima energy levels gives rise to a change in the carrier concentrations in the conduction band. In silicon, for example, the density of electrons associated with the six conduction band minima is given by

$$n = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2} \{m_{C1}^{3/2} \exp[-(\frac{E_{C1} - E_F}{kT})] + m_{C2}^{3/2} \exp[-(\frac{E_{C2} - E_F}{kT})] + m_{C3}^{3/2} \exp[-(\frac{E_{C3} - E_F}{kT})]\} , \quad (5)$$

where E_F = the Fermi energy level, and m_{Ci} = the effective electron masses associated with the energy minima. Equation (5) can be rewritten as

$$n = \frac{n_o}{3} \exp(\frac{\Delta E_F}{kT}) \left[\exp(-\frac{\Delta E_{C1}}{kT}) + \exp(-\frac{\Delta E_{C2}}{kT}) + \exp(-\frac{\Delta E_{C3}}{kT})\right] , \quad (6)$$

where n_o = unstressed electron density, and ΔE_F = change in the Fermi level. Similarly, the carrier concentration associated with the valence band maxima is given by

$$p = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2} \{m_{V1}^{3/2} \exp[-(\frac{E_F - E_{V1}}{kT})] + m_{V2}^{3/2} \exp[-(\frac{E_F - E_{V2}}{kT})]\} \quad (7)$$

where m_{Vi} = effective masses associated with the valence band maxima, E_{Vi}. In Eq. (7), the Γ'_{25} (j = 1/2) energy level has been neglected. If the small difference between m_{V1} and m_{V2} is also neglected, a good approximation for silicon, Eq. (7) can be written as

$$p = \frac{p_o}{2} \exp(-\frac{\Delta E_F}{kT}) \left[\exp(\frac{\Delta E_{V1}}{kT}) + \exp(\frac{\Delta E_{V2}}{kT})\right] , \quad (8)$$

where p_o = the hole concentration with no stress.

The $\exp(-\frac{\Delta E_F}{kT})$ terms in Eqs. (6) and (8) can be evaluated by setting the majority carrier density equal to the impurity density and assuming the ionization energy to be independent of stress. Consequently, the hole density remains constant in p-type material, for example, and

$$\exp(\frac{\Delta E_F}{kT}) = \frac{1}{2} \left[\exp(\frac{\Delta E_{V1}}{kT}) + \exp(\frac{\Delta E_{V2}}{kT})\right] . \quad (9)$$

Substituting Eq. (9) into (6) yields the ratio of stressed to unstressed minority carrier density, $\gamma_\nu(e)$, in the p-type material as (Ref. 3)

$$\gamma_\nu(e) = \frac{n_p}{n_{po}} = \frac{1}{6}\left[\exp\left(\frac{\Delta E_{V1}}{kT}\right) + \exp\left(\frac{\Delta E_{V2}}{kT}\right)\right]\left[\exp\left(-\frac{\Delta E_{C1}}{kT}\right) + \exp\left(-\frac{\Delta E_{C2}}{kT}\right) + \exp\left(-\frac{\Delta E_{C3}}{kT}\right)\right] . \quad (10)$$

Following a similar procedure for n-type material, it can be shown that (Ref. 3)

$$\frac{p_n}{p_{no}} = \frac{n_p}{n_{po}} = \gamma_\nu(e) . \quad (11)$$

Deformation Potential Coefficients

The deformation potential coefficients have been evaluated both theoretically and experimentally, and the values used herein are underlined in Table I. It is possible that the deformation potential coefficients change with doping. In particular, the value D_u' is uncertain, however, the value of 2.68 eV/unit dilation appears to be the better value from experimental observations. The function $\gamma_\nu(e)$ has been calculated using the above value of D_u'.

Calculated Values of $\gamma_\nu(e)$

The ratio of stressed to unstressed minority carrier density, $\gamma_\nu(e)$, has been calculated for hydrostatic and uniaxial [100], [011] and [111] tensional and compressional stresses. Figures 3 and 4 are plots of $\gamma_\nu(e)$ as a function of compressional and tensional stresses, respectively, for $D_u' = 2.68$. For a hydrostatic and uniaxial [100] stress, $\gamma_\nu(e)$ is independent of D_u'. The exponential increase in $\gamma_\nu(e)$ with stress in a basic characteristic of the piezojunction phenomenon. It is evident from Fig. 3 $\gamma_\nu(e)$ is most sensitive to a [100] compressional stress, and least sensitive to a [111] tensional stress. It is also evident that the piezojunction effect is significant at stress levels greater than 10^9 dynes/cm^2; i.e., order-of-magnitude changes occur in $\gamma_\nu(e)$ with changes in stress. The mechanical strength of silicon limits the stress that can be applied to a p-n junction in silicon and is the basic limitation to changes that can be achieved in $\gamma_\nu(e)$. The fracture strength

Table I. (Ref. 5)

Deformation Potential Coefficients (eV/unit dilation) for Si. (Kleinman's theoretical values are shown in brackets. Values used in this investigation are underlined.)

Coefficient	Si
D_d	[- 2.09]
D_u	2.04,[a] [3.74]
D'_u	2.68,[a] 10,[e] [4.23]
Ξ_d	[- 4.99]
Ξ_u	11,[b] 8.3,[c] [+ 9.6]
$D_d - (\Xi_d + \frac{1}{3}\Xi_u)$	- 1.44,[d] [- 0.30]

a J. C. Hensel and G. Feher, Phys. Rev. 129, 1041 (1963).

b D. K. Wilson and G. Feher, Phys. Rev. 124, 1968 (1961).

c J. E. Aubrey, W. Gubler, T. Henningsen, and S. H. Keonig, Phys. Rev. 130, 1667 (1963).

d W. Paul, J. Phys. Chem. Solids 8, 196 (1959).

e J. J. Wortman, Private Communication.

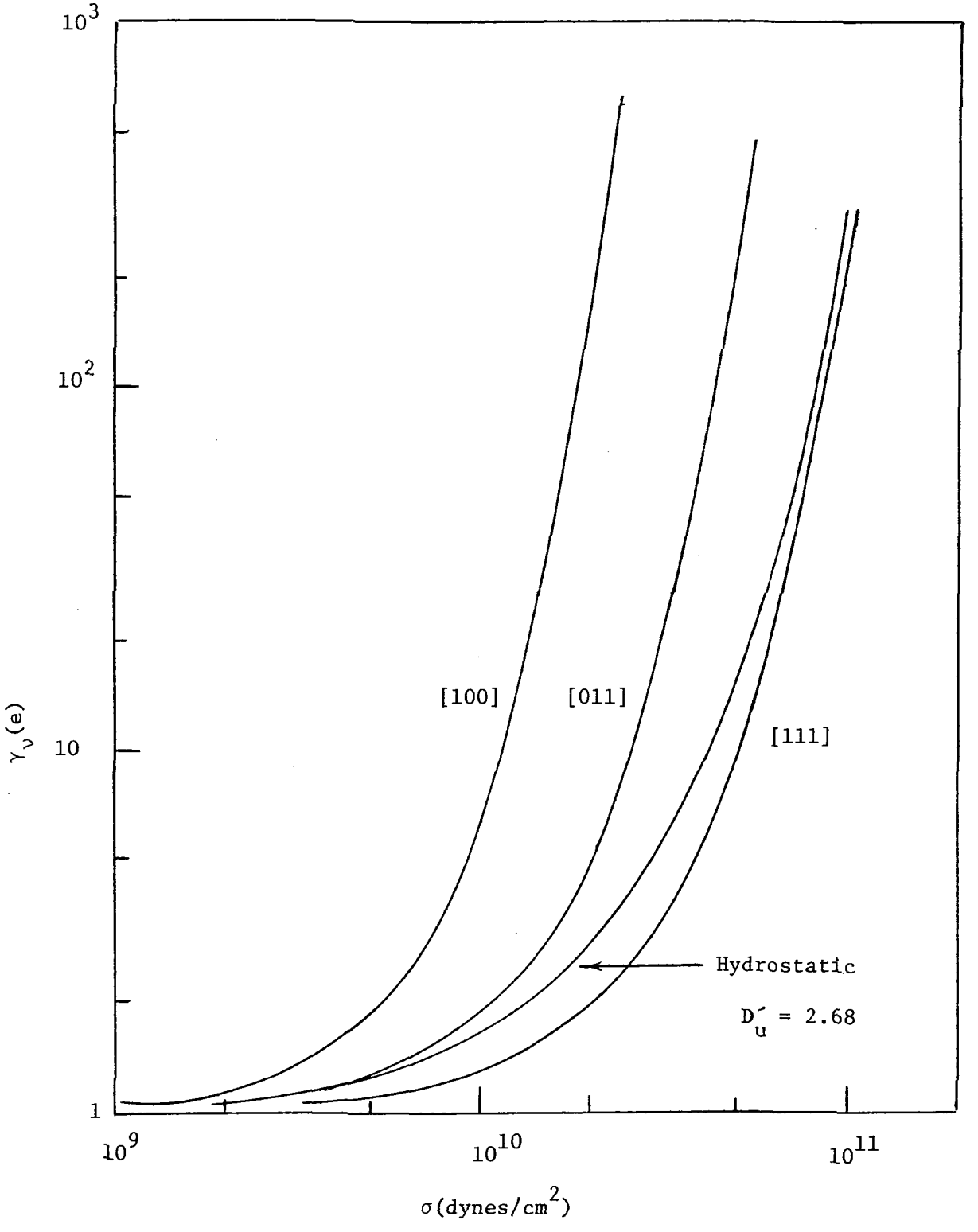


Figure 3. Ratio of Stressed to Unstressed Minority Carrier Density for a Hydrostatic, [100], [011] and [111] Uniaxial, Compressional Stress

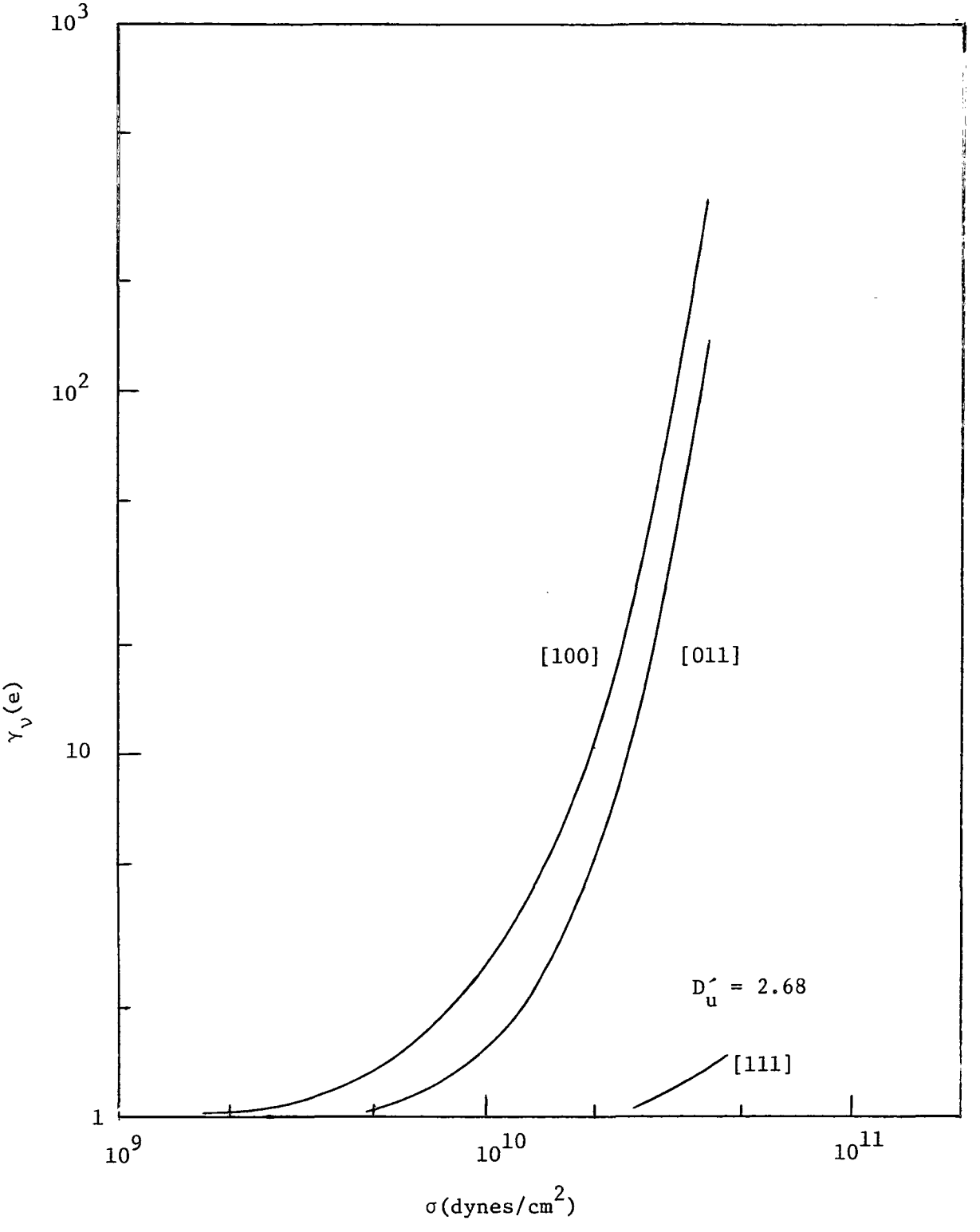


Figure 4. Ratio of Stressed to Unstressed Minority Carrier Density for a [100], [011] and [111] Uniaxial, Tensional Stress

of silicon varies from sample to sample and depends to a large extent on the surface conditions (Ref. 7). However, order of magnitude changes have been experimentally observed in $\gamma_\nu(e)$.

Effect of Stress on p-n Junction Characteristics

The effect of stress on p-n junction characteristics has been described by Wortman, et al., in terms of $\gamma_\nu(e)$. Changes in other parameters are assumed to be negligible as compared with the exponential change of $\gamma_\nu(e)$ with stress above 10^9 dynes/cm^2. This model also neglects the contribution of surface generation-recombination currents.

The total current (I) in p-n junctions is the sum of the ideal current (I_I) and the generation-recombination currents (I_R).

$$I = I_I + I_R \ . \tag{12}$$

For forward biased conditions, the bulk generation-recombination current is given approximately by

$$I_R = \frac{a\ \gamma_\nu(e)\ [\exp(qV/kT) - 1]}{1 + b\ \sqrt{\gamma_\nu(e)}\ \exp(qV/kT)} \ , \tag{13}$$

where a and b are device constants. The ideal current is given by

$$I_I = c\ \gamma_\nu(e)\ [\exp(qV/kT) - 1] \ , \tag{14}$$

where c is a device constant. Equation (12) becomes (Ref. 4)

$$I = \frac{a\ \gamma_\nu(e)\ [\exp(qV/kT) - 1]}{1 + b\sqrt{\gamma_\nu(e)}\ \exp(qV/2kT)} + c\ \gamma_\nu(e)\ [\exp(qV/kT) - 1] \ . \tag{15}$$

It is of interest here to consider the p-n junction current under different bias conditions. For large forward biases, Eq. (15) is approximately

$$I \simeq \frac{a}{b}\ (\gamma_\nu(e))^{1/2}\ \exp(qV/2kT) + c\ \gamma_\nu(e)\ \exp(qV/kT) \ . \tag{16}$$

It is significant that for large forward biases; i.e., V > 0.3 volts, p-n junction current will have a larger dependence on the ideal component of current than the generation-recombination component. For reverse-bias conditions the ideal current is much less than the generation-recombination current. The effects of stress on the generation-recombination current in the reverse-biased mode is not easily described. Experimentally, reverse-biased p-n junctions have been observed to be very sensitive to stress and relatively independent of voltage for voltages less than the breakdown voltage. The forward-biased characteristics, as shown in Eq. (16) are dependent upon $\gamma_\nu(e)$ and the applied voltage.

Hauser and Wortman (Ref. 5) have also investigated the effect of mechanical stress on the breakdown voltage of p-n junctions and, in the case of silicon, found the change in breakdown voltage to be

$$\frac{\Delta V}{V_B} \approx - (10^{-12}\ \text{cm}^2/\text{dyne})\ \sigma \qquad (17)$$

where σ is the applied stress, ΔV is the change in breakdown voltage and V_B is the unstressed breakdown voltage. The change in breakdown voltage is also independent of orientation. Since the breakdown voltage is a linear function of stress whereas the junction current at a voltage less than breakdown voltage is an exponential function of stress, the latter mode of operation is potentially a more sensitive transducing mechanism. However, if voltage is held constant across the device in the breakdown region, current can change greatly with small voltage changes. Breakdown voltage is also less sensitive to temperature changes than junction currents, and this mode of operation may have advantages in some applications.

The effects of stress on more complex silicon p-n junction structures is also of interest. Wortman, et al., has investigated the effects of stress upon transistor characteristics and p-n-p-n switches (Ref. 3). If both sides of the emitter-base junction of a transistor are stressed, the base and collector currents are changed several orders of magnitude for small changes in stress above 10^{10} dynes/cm^2. The current gain will not be affected if both junctions are similarly stressed. If only the emitter side of the junction is stressed ($e_e >> e_b$) the base current increases orders of magnitude with stress while the collector current remains unchanged. Consequently, gain is reduced by stressing the emitter side of the base-emitter junction. If only the base side of the junction is stressed ($e_e << e_b$), the base and collector currents remain approximately the same.

Calculations of Sensitivity for Mesa Devices

It will be assumed that only forward-biased diodes will be used. This assumption eliminates considerations of the unknown behavior of reverse-biased p-n junctions. From a fabrication point of view it is very difficult to construct devices for sensor applications in a predictable and consistent manner whose reverse I-V characteristics are reproducible. This is a direct result of a dominating generation-recombination current in the reverse-biased mode for silicon devices. For discussion purposes, a second assumption will also be made which is only diodes whose forward-biased I-V characteristics are of the "ideal" or Shockley type will be considered; i.e., no generation-recombination current components ($I_R << I_I$). In practice this will require forward-biased voltages on the order of 0.3 volts or greater. Imposing this requirement will insure that only devices with known and well-understood characteristics are used. It automatically will eliminate hysteresis effects which could result from trapping effects and hence influence the piezojunction effects. That is, the characteristics will not be a function of generation-recombination centers in the material which could be influenced by stress.

Using the above assumptions, the simple piezojunction theory based on deformation potential theory is applicable. For the simple geometry in which the total stressed area is the total junction area, A, and large forward bias, the current-voltage characteristics are related to stress through γ,

$$I = I_o \gamma(\sigma) e^{qV/kT} , \tag{18}$$

where the assumption has been made that $e^{qV/kT} >> 1$.

In the case where only a part of the junction is stressed, A_s, the current can be accounted for by considering two parallel components

$$I = I_o \left(\frac{A_s}{A} \gamma(\sigma) + \frac{A - A_s}{A}\right) e^{qV/kT} . \tag{19}$$

Equation (19) assumes that both the stressed and unstressed portions of the junction have equal voltages applied. A second assumption which is implied in Eq. (19) is that the stressed area is independent of the applied stress; i.e., $A_s \neq f(\sigma)$.

For the case of a flat top mesa, Eq. (19) will hold. Figure 5 shows plots of $\Delta I/I$ as a function of stress for a [100] oriented sample with various A_s/A ratios.

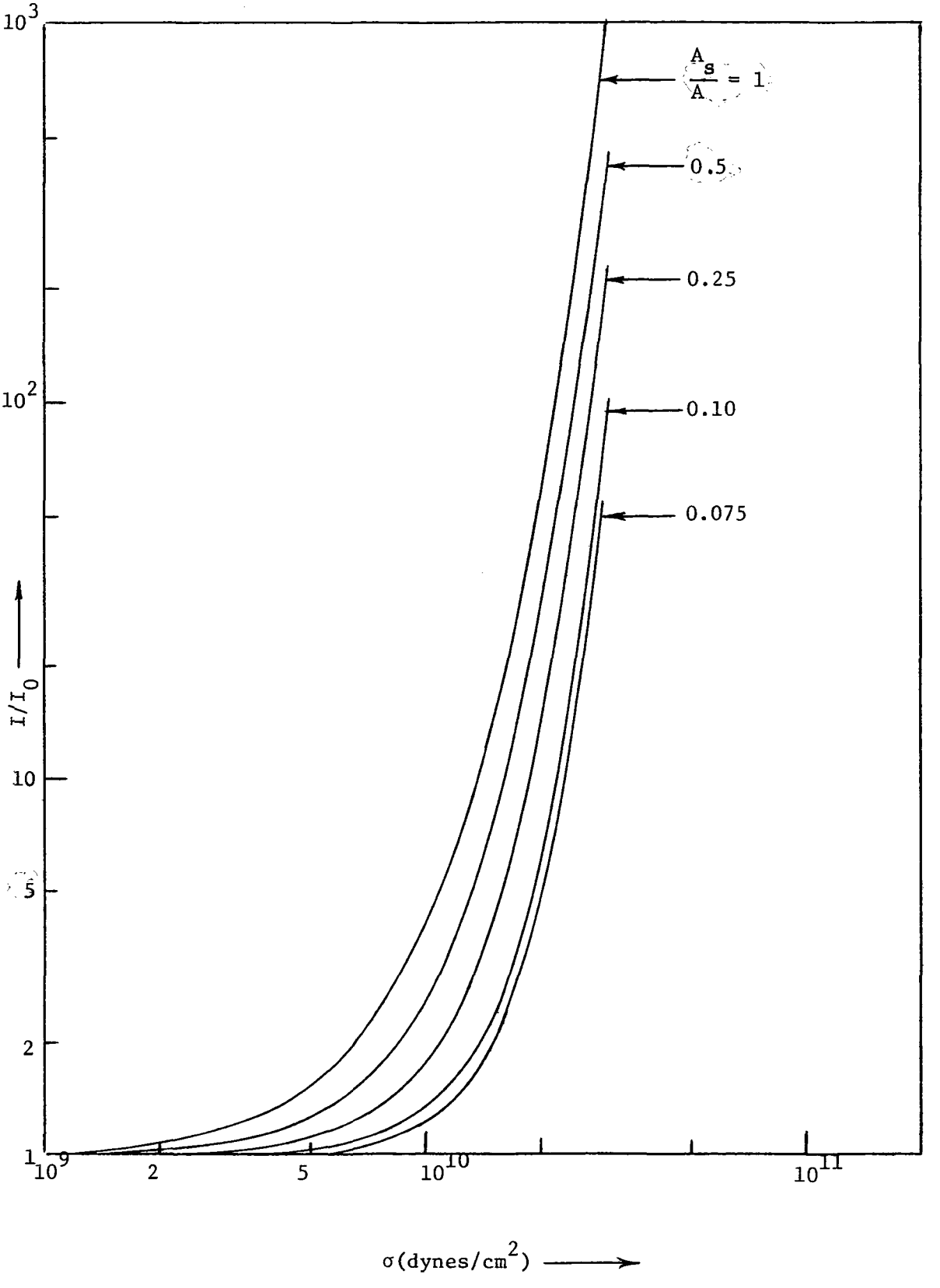


Fig. 5. I/I_0 Versus Stress (σ) for Various Ratios of Stress Area To Total Area (A_s/A).

Spreading resistance problem. - The effects of spreading resistance, R, in p-n junctions can be accounted for by considering the resistance to be in series with the diode. This assumption allows the linear summation of the voltages; i.e.,

$$V_a = V + V_R \ , \tag{20}$$

where V is the diode voltage, V_R is the voltage dropped in the diode other than that across the junction, and V_a is the applied voltage. The current equation for the diode is, therefore, modified as follows

$$I = I_o \left(e^{q(V_a - IR)/kT} - 1\right) \ , \tag{21}$$

where $V_R = IR$.

As shown by Eq. (21), the spreading resistance is important when IR is comparable to the applied voltage. If the junction is operated at a current level such that the spreading resistance is important it will reduce the stress sensitivity of a junction if the junction is operated with a fixed forward voltage. The spreading resistance of a junction can be calculated using the resistivity expression $R = \rho\ell/A$, where ℓ and A are effective values. The current through the unstressed part of the junction, I_U, is

$$I_U = I_o \left(\frac{A - A_s}{A}\right) \exp q(V_a - I_U \rho\ell/[A - A_s])/kT \tag{22}$$

and that through the stressed part, I_s, is

$$I_s = I_o \frac{A_s}{A} \gamma(e) \exp q(V_a - I_s \rho\ell/A_s)kT \ . \tag{23}$$

The total current is

$$I = I_s + I_U \ . \tag{24}$$

As is easily seen by combining Eqs. (22) - (24), the current-voltage characteristics are very complex functions of stress. The problem is not as impossible to handle as it may at first appear. For example, I_U is unaffected by stress and it can be easily estimated in a practical case by measuring I_o and taking the ratio of A_s/A at a bias level such that the spreading resistance is not important.

The spreading resistance in the unstressed case, R_o, can be determined from an I-V plot. Once it is obtained one can estimate R_U and R_s by the following equations

$$R_o = \frac{\rho \ell}{A} \tag{25}$$

$$R_U = \frac{R_o A}{A - A_s} \tag{26}$$

$$R_s = \frac{R_o A}{A_s} \tag{27}$$

Figure 6 shows the effect of spreading resistance on the V-I characteristics of a typical laboratory junction with various values of spreading resistance. As shown in Fig. 6, one would be limited to current magnitudes less than 10^{-5} amperes if the spreading resistance is unavoidable. The effect of a 50 ohm spreading resistance in the unstressed case is shown in Fig. 7 for a $\gamma(e)$ of 10^3. Note the various area effects. For the A_s/A ratio of 0.1 a practical current limit of 10^{-5} would be the upper value for a sensor current if spreading resistance effects were to be avoided.

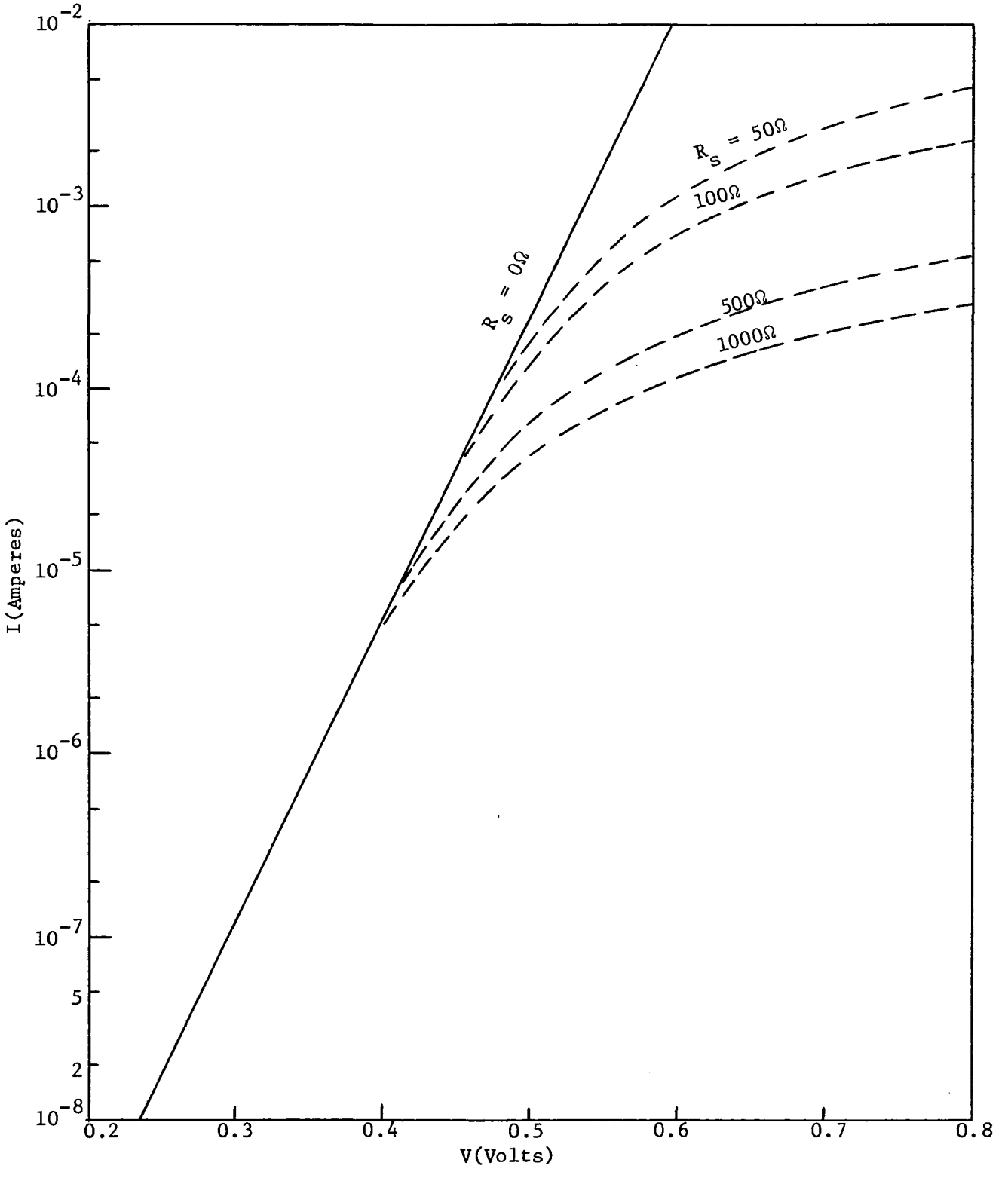


Fig. 6. An Illustration of the Effects of Spreading Resistance.

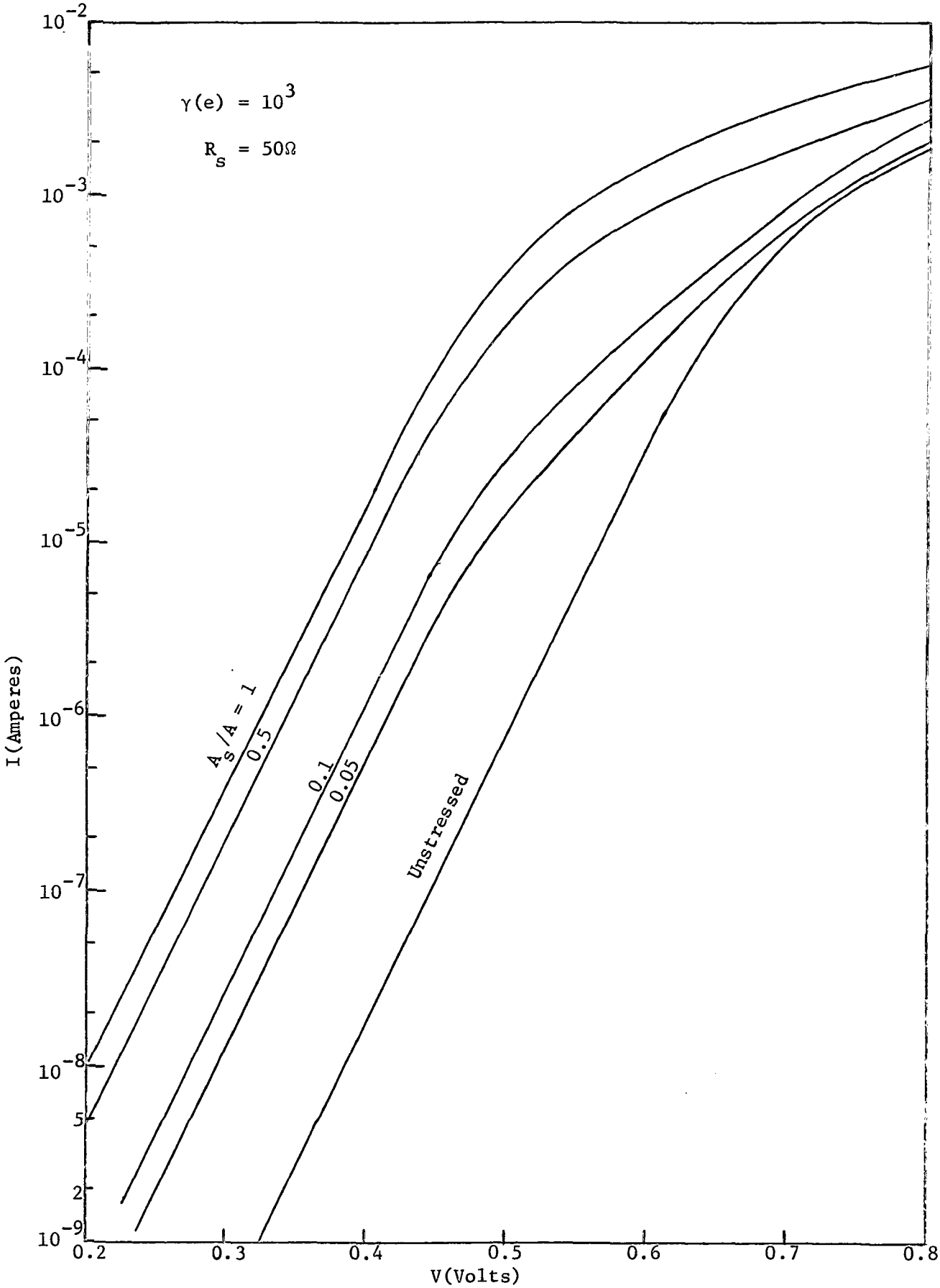


Fig. 7. The Combined Effects of Spreading Resistance and Stressed Area to Total Area Ratios.

SECTION III

TRANSDUCER DESIGN CONSIDERATIONS

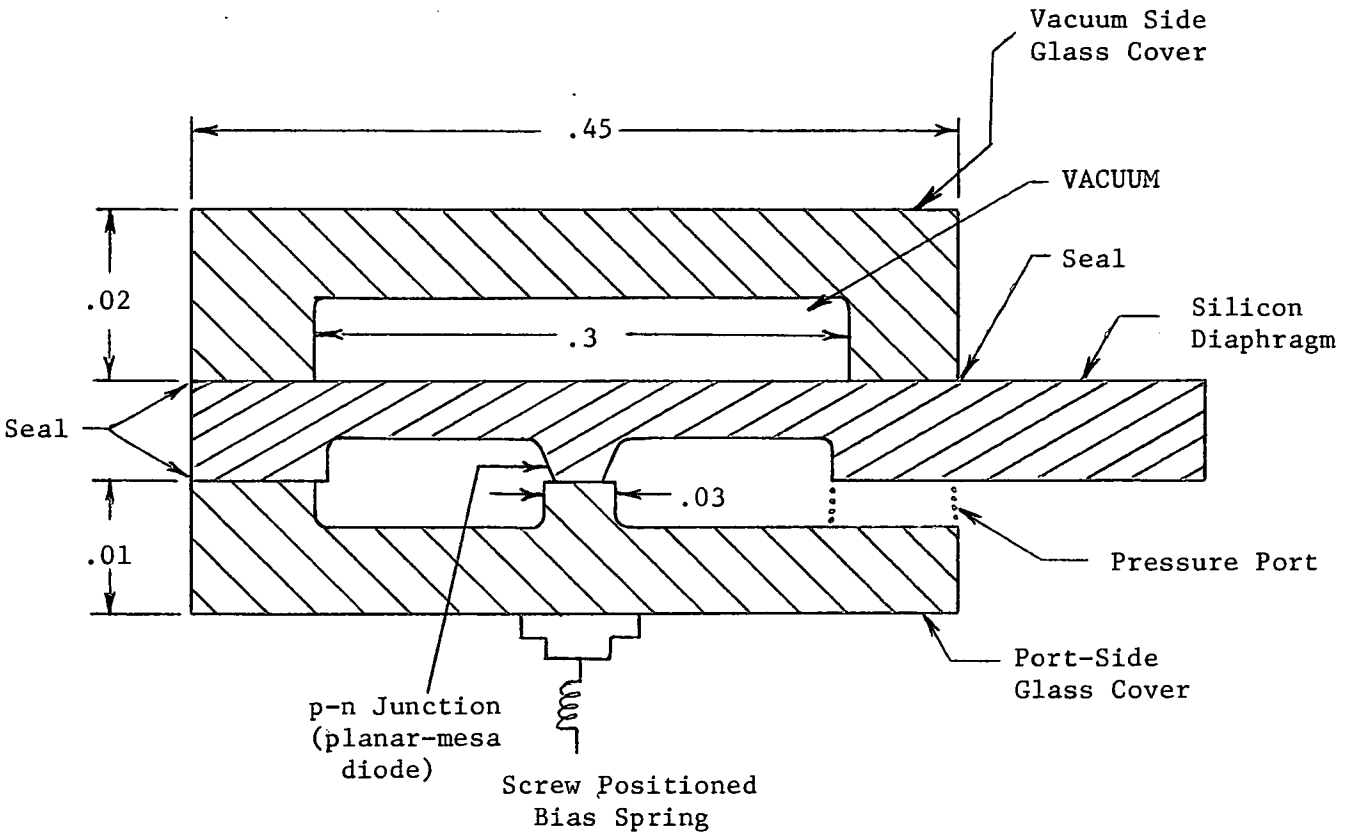
Junction Element

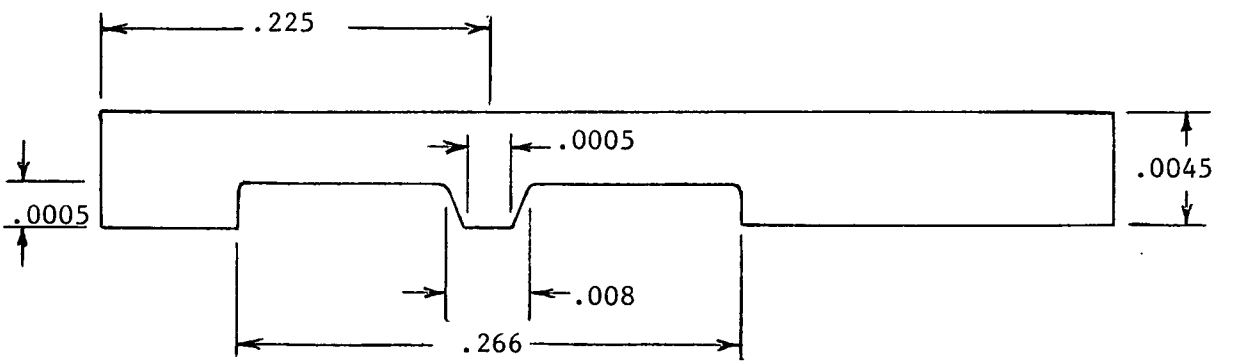
A practical pressure transducer based on the piezojunction effect will be heavily dependent on the solid-state semiconductor technology. The sensing junction configuration, geometry, dimensions and electrical properties are all limited to the state-of-the-art semiconductor processes. Within this technology and a knowledge of the theory and experimental data on the piezojunction effect, a mechanical system must be devised to utilize the effect in a practical manner. An evolutionary process has lead to a mechanical configuration which utilizes a planar-mesa diode fabricated on a silicon diaphragm as the sensor element. A glass wafer containing a cavity for a vacuum reference has evolved as the pressure element on one side of the silicon diaphragm, and a glass pressure plate is used on the opposite of the vacuum to apply stress to the sensing junction. Figure 8 is a sketch of this basic system.

Based on the semiconductor technology, which is discussed in Sect. IV of this report, it was estimated that the smallest mesa area which could be reproducibly fabricated in the RTI laboratory was on the order of 1/4 square mils. The smallest total diode area which would not cause the junction to fall on the side of the mesa and would allow for contacts to the junction was on the order of 1.25 square mils. Based on these numbers, a stressed to unstressed area ratio of 0.175 was selected as a practical limit. It is, of course, very desirable to increase this ratio as much as possible for reasons discussed in Sect. II. Using the above ratio value, a stress magnitude is required which will change the current through the stressed area by a factor of approximately ten before any significant change is observed in the total junction current. Figure 9 is a theoretical sketch of I/I_0 as as a function of stress for the stressed area to total area ratio $(\frac{A_s}{A})$ of 0.175. Note the straight line in Fig. 9 above 2×10^{10} dynes/cm^2. The task is to design a transducer which utilizes this sensitivity in a practical configuration to measure the desired pressure.

Capsule Design

Analysis of the Design. - The following is a discussion of the design of the capsule diode illustrated in Fig. 8. To begin, consider a silicon diaphragm with fixed edges and with a uniform load applied as shown in Fig. 10. The deflection y, of the center of the diaphragm is given by





Silicon Diaphram Dimensions

(all dimensions in inches)

Figure 8. An Illustration of the Capsule Diode

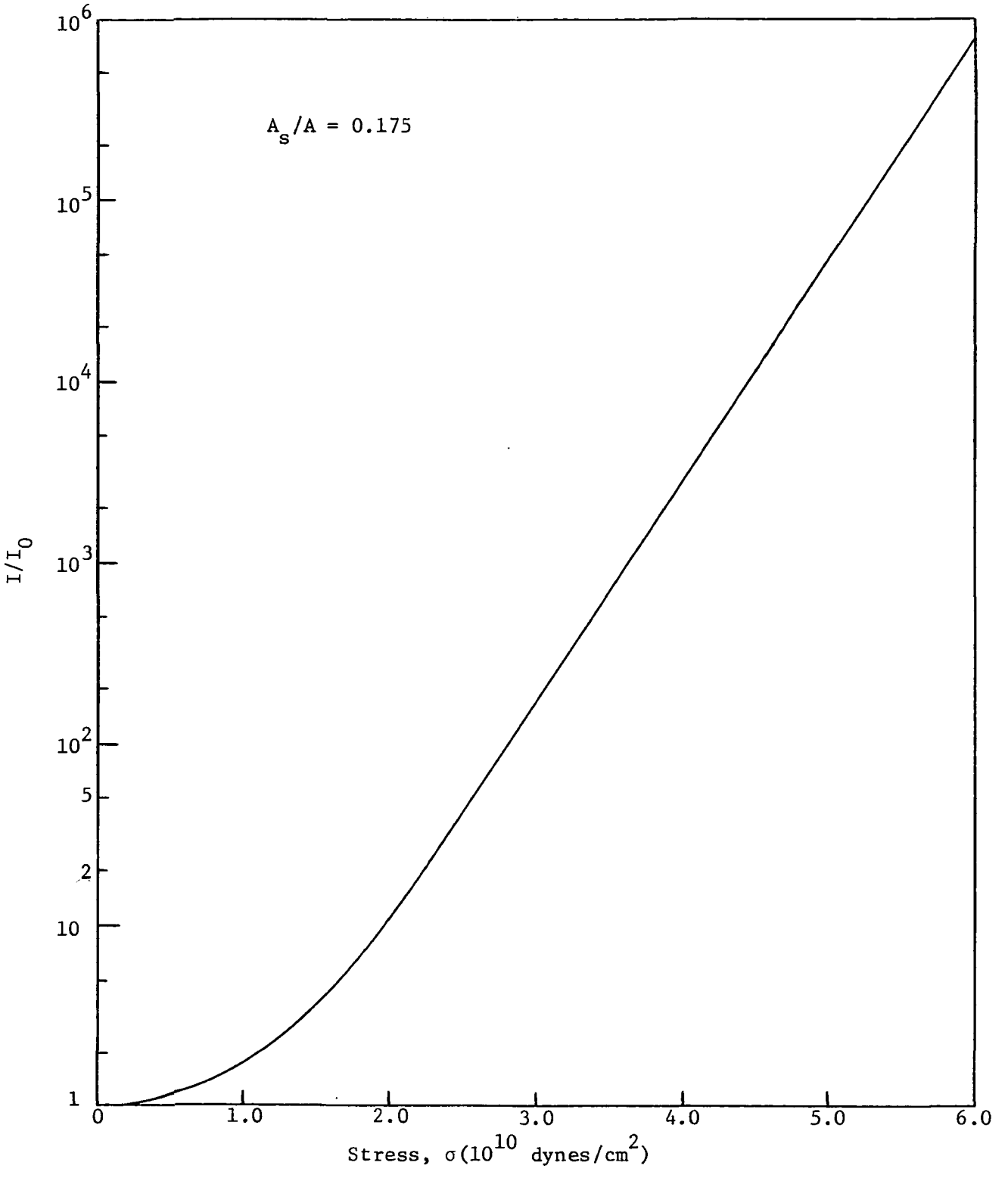


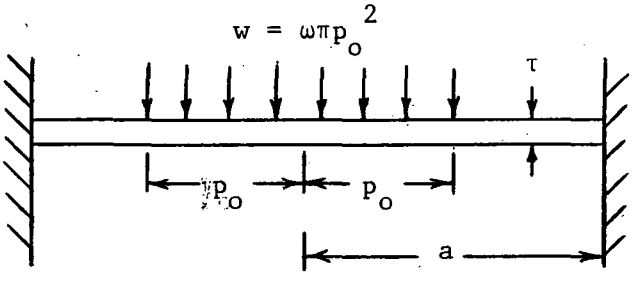
Fig. 9. I/I_0 Versus Stress for an A_s/A Ratio of 0.175.

$$y = \frac{-3W(m^2-1)}{16\pi\ E\ m^2 t^3}\left[4a^2 - 4r_o^2 \log \frac{a}{r_o} - 3r_o^2\right] \qquad (28)$$

where m is the reciprocal of Poisson's ratio and E is Young's modulus (Ref 8). For small values of r_o such that the load is a concentrated load, the deflection is

$$y = \frac{-3W(m^2-1)a^2}{4\pi\ E\ m^2 t^3} \quad . \qquad (29)$$

These equations are good only for small deflections; i.e., no ballooning. Using Eq. (28) and Eq. (29) and the principle of superposition, it can be shown that if the center of the diaphragm is held fixed by a support on one side and a uniform load on the other side, the center support will carry 1/5 of the total load. The remaining 4/5 of the uniform load will be carried by the fixed edges of the diaphragm.



ω = uniform load (force/area)

Fig. 10. A Fixed Diaphragm, Uniformly Loaded.

Assume the silicon diaphragm of Fig. 10 to have the dimensions of the diaphragm in Fig. 8, i.e., a thickness (t) of 5 mils and a diameter of 270 mils. An atmosphere of pressure would cause a deflection of 13 mils. (This value was calculated using a value of 2.17×10^{10} lb/in^2 for Young's modulus and 0.25 for Poisson's ratio.) If the silicon diaphragm has a mesa supported by a fixed post such as the port-side glass wafer of Fig. 8, the silicon mesa would experience a force of 0.21 lb or 9.3×10^4 dynes with one atmosphere of pressure applied. If the silicon mesa has an area of 1/4 square mil, a force of 9.3×10^4 dynes will yield a stress of 5.8×10^{10} dynes/cm^2.

Consider next the complete capsule diode of Fig. 8. If the glass post is caused to contact the silicon mesa when the pressure is one atmosphere, the mesa would be stressed to 5.8×10^{10} dynes/cm^2 when the pressure was zero. At some pressure between an atmosphere and zero, the diode would be stressed at 2×10^{10} dynes/cm^2, for example. (This value was selected from the linear portion of Fig. 9.) The lower the pressure at which this value of stress occurs, the greater will be the sensitivity of the capsule diode at low pressures. A worst-case condition could be for a stress of 2×10^{10} dynes/cm^2 to correspond to an atmosphere of pressure.

Referring again to the capsule diode structure of Fig. 8, the stress applied to the diode can be expressed as

$$\sigma = C_1 - C_2 P \tag{30}$$

where C_1 and C_2 are constants and P is the applied pressure. Assuming the worst-case conditions of the preceeding paragraphs; when P is zero, σ is 5.8×10^{10} dynes/cm^2, and when P is 760 mm Hg, σ is 2×10^{10} dynes/cm^2. It follows that C_1 is 5.8×10^{10} dynes/cm^2 and C_2 is 5×10^7 dynes/cm^2/mm Hg. Equation (30) becomes

$$\sigma = 5.8 \times 10^{10} \text{ dynes/cm}^2 - 5 \times 10^7 \text{ dynes/cm}^2\text{/mm Hg} . \tag{31}$$

Combining Eq. (31) with the curve in Fig. 9 (or with Eq. (19)), the following expression is obtained for the current as a function of pressure

$$I/I_0 \simeq 8.8 \times 10^5 \exp\left(-1.5 \times 10^{-2} \text{ P/Torr}\right) . \tag{32}$$

Figure 11 is a plot of Eq. (32) in which I/I_0 at P = 0 has been chosen as the normalizing factor. Note that the relative change in current per unit pressure is

$$\frac{\Delta I}{I} / \Delta P \simeq 1.5 \times 10^{-2}/\text{Torr} . \tag{33}$$

A change in pressure of 10^{-2} Torr would result in a relative current change of 1.5×10^{-4}. This small change would be difficult to detect.

If no mechanical bias were applied to the junction such that the stress was zero at 760 Torr, then

$$\frac{\Delta I}{I} / \Delta P \simeq 2.2 \times 10^{-2}/\text{Torr} . \tag{34}$$

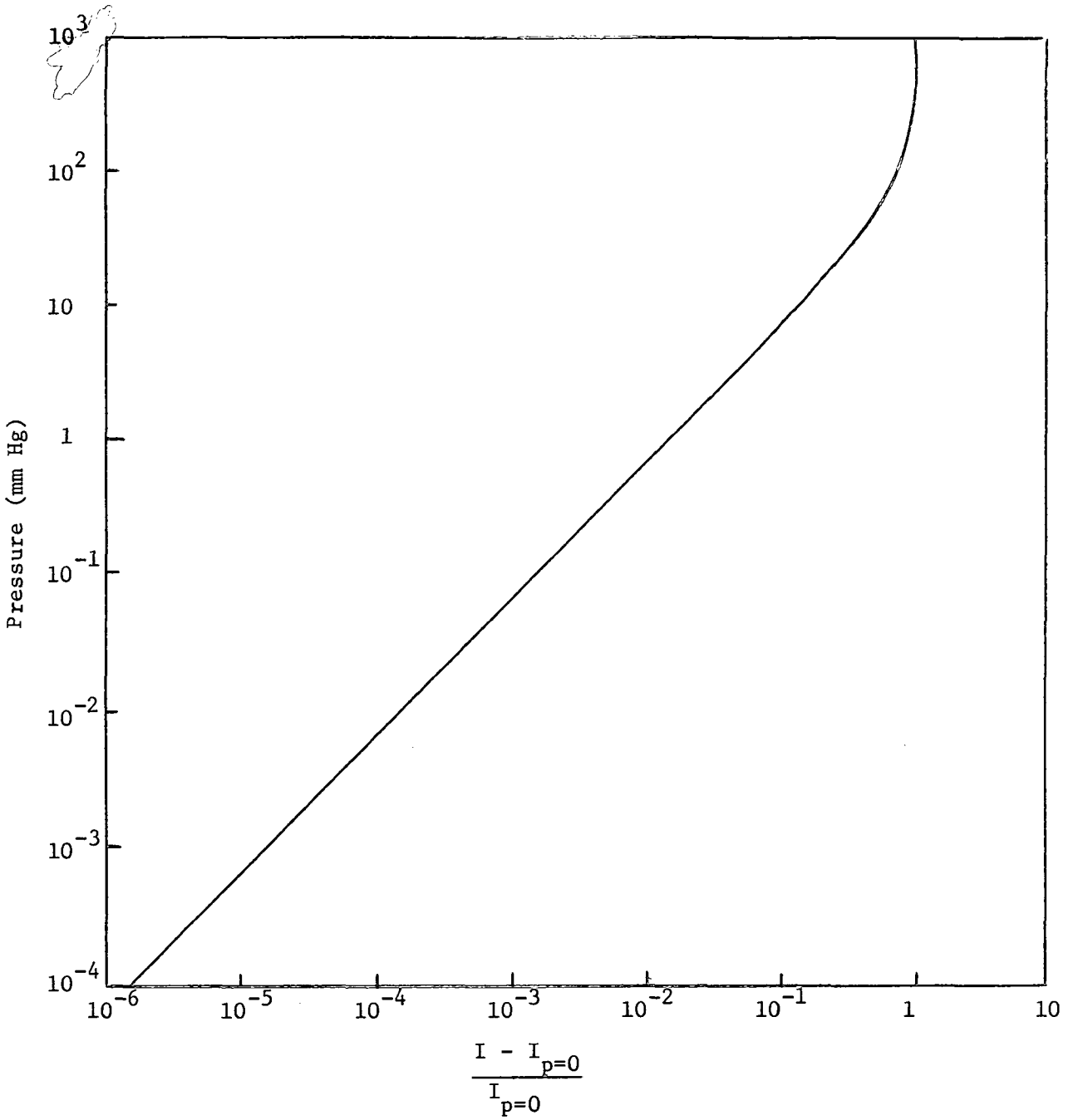


Fig. 11. Relative Change in Current Per Unit Pressure.

Another possibility is to fix the diaphragm system such that no pressure is applied to the junction until some reduced pressure level is reached such as 100 Torr. For this case

$$\sigma = 0;\ P > 100 \text{ Torr}$$

$$\sigma = (6 \times 10^{10} - 6 \times 10^{8}\ P/\text{Torr})\ d/cm^2;\ P < 100 \text{ Torr}. \qquad (35)$$

This yields a significantly improved sensitivity as shown in Eq. (36).

$$\frac{\frac{\Delta I}{I}}{\Delta P} \simeq 1.7 \times 10^{-1}/\text{Torr}. \qquad (36)$$

Performance Limits

The transducers fabricated during this program were disappointing in that sensitivity goals were not achieved and, of more significance, the transducers were not repeatable (See Sect. VI). A basic limit to performance was the poor quality of the planar-mesa diodes fabricated. Surface and/or generation-recombination currents were characteristic of most of the diodes, and excessive spreading resistance limited the diodes to undesirably low voltage biases. These limiting factors have been discussed previously. Others are discussed in the following paragraph.

Moving Diaphragm Problem. - The capsule diode configuration of Fig. 8 is theoretically stable with a unique value of force (stress) applied to the diode for a given pressure and initial bias value. It is a complex mechanical system, however, that apparently fails to provide adequate stability. It is difficult, for example, to obtain a smooth control of the initial stress with the screw adjustment, and simply touching the bias screw has a noticeable effect on the diode characteristics.

The complexity of the system is apparent if the various diaphragms are represented as springs. The resulting system consists of three seried springs, one end fixed (hopefully) by the position of the bias adjust screw and the other acted upon by a force proportional to pressure. It is suggested that subsequent designs eliminate some of this complexity. If the port-side glass cover could be clamped in a fixed position relative to the vacuum-side cover, for example, the system would be considerably less complex consisting of a single spring (diaphragm) and a force proportional to pressure. Since the initial stress-bias is not critical, one method would be to fix the position of the port-side glass with epoxy after the bias is set. A second method would contact a larger area of the port-side cover directly with the bias adjust screw. If the screw were fabricated from the ceramic material used to fabricate this housing, additional temperature stability would be gained (See Sect. V). After stress-biasing, the position of the screw could be fixed with epoxy.

SECTION IV

SEMICONDUCTOR PROCESSING

The processing philosophy followed during this investigation differs in detail from that of the predecessor contract, NAS1-7489, in that the silicon shape chosen for fabrication is more compatible with the standard processing methods of the highly developed planar silicon technology. Under the preceding program, the silicon was shaped into a needle-like rod and the p-n junction was fabricated on the tip of this needle. The chief problems of this approach were the difficulty in defining the region of the p-n junction on the tip of the needle and, once having defined the junction area, making contact to both sides of the junction. The present design configuration--the planar-mesa approach--is an attempt to retain the sensitivity of the needle configuration and, at the same time, simplify the fabrication over that required for the needle approach.

Planar Mesa Technology

A brief history and background of the planar-mesa technology as well as an outline of its essential features are given in Ref. 9. The description given in Ref. 9 serves as a starting point for the development carried out under the present contract.

A cross section of the planar mesa in the capsule diode configuration is sketched in Fig. 12. This structure employs the planar-mesa as the stress sensitive element and incoporates several other noteworthy features as well: 1) the use of the Mallory Electrostatic Sealing Process to effect a hermetic seal around the periphery of the silicon diaphragm. If the sealing operation is carried out in a vacuum, the cavity between the glass lid and the silicon chip containing the pressure sensitive mesa is effectively a zero reference of pressure. 2) the use of a single planar-mesa (as opposed to a previously employed tri-mesa configuration) which is loaded by a self-aligned mesa in the opposing glass lid. The matching edges of the silicon chip and the glass lid serve to align the glass mesa with the silicon mesa in a parallel, mechanically stable position.

The assembly of this structure is summarized as follows:

1) The planar-mesa diode is diffused and etched as described in Section V.

2) A vacuum-side glass wafer, etched to the general configuration illustrated in Fig. 12, is anodically sealed to the silicon diaphragm by the electrostatic sealing process described by Pomerantz and others at Mallory (Ref. 10). This sealing process is carried out inside a vacuum chamber at a pressure of approximately 10^{-5} torr.

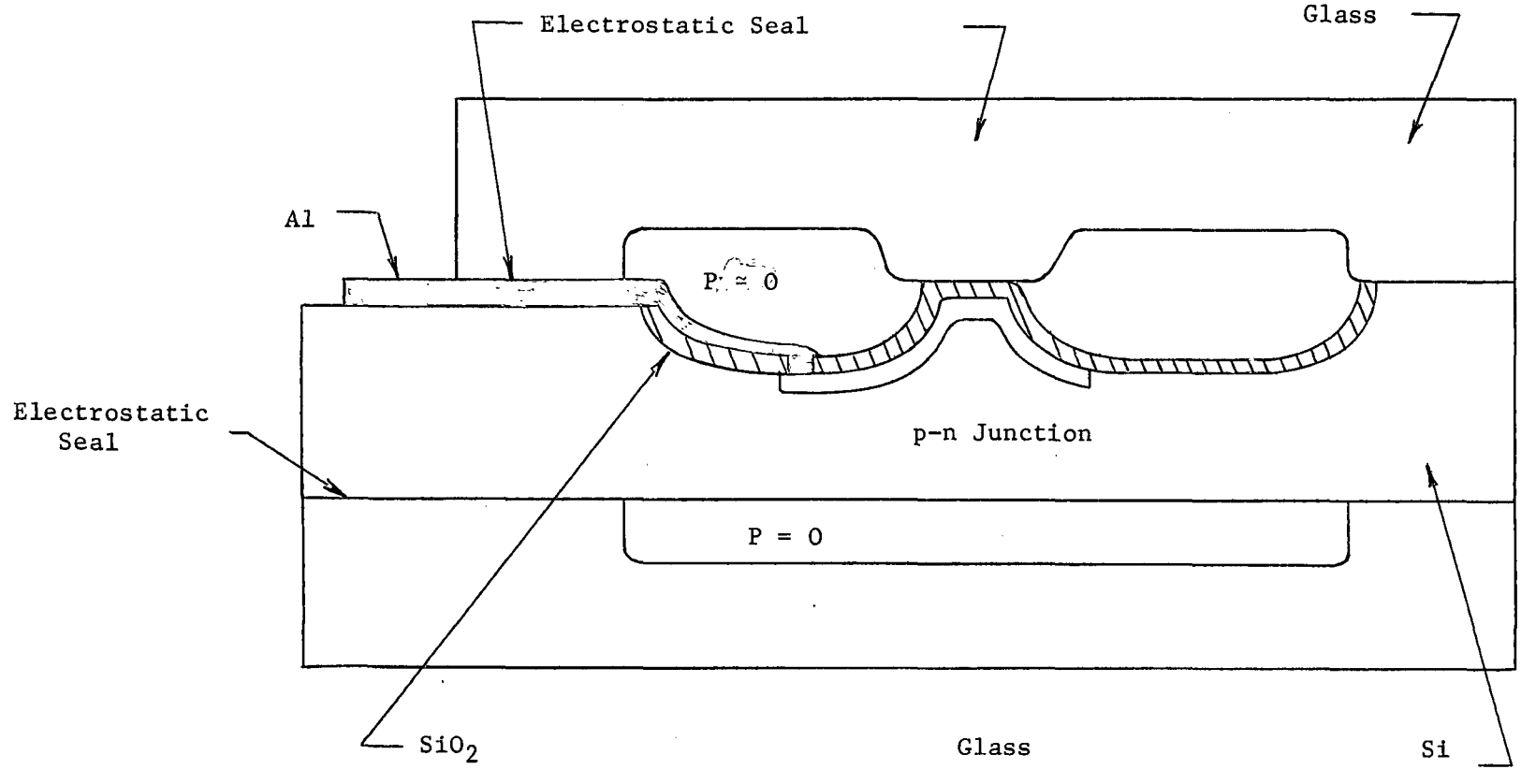


Figure 12. Final Capsule Diode Design

3) Finally, the port-side glass wafer is sealed to the diode-side of the silicon diaphragm. This seal is carried-out in an atmosphere of pressure and features a pressure-port into the cavity. In this design, the vacuum reference deflects the silicon diaphragm away from the glass mesa that serves as a stress-plate for the planar-mesa diode. At an atmosphere, for example, the diode may not be stressed or may not even contact the port-side wafer. As pressure decreases, the force on the diode increases.

An earlier design is illustrated in Fig. 13. This design used a single glass wafer, required a single seal, and the diode was located in the vacuum reference cavity. This design required an anodic seal over a surface supporting the metallization stripes, and this was frequently troublesome. A more significant difficulty was that the diode was at maximum stress at ground level or one atmosphere of pressure.

Fabrication Critique

While the schemes outlined above for fabricating and housing piezo-junction diodes are quite compatible with standard planar processing, various problems did arise during fabrication. These problems are discussed briefly in the following paragraphs.

Pinholes in the oxide. - The first major problem in fabrication arose when making a planar-mesa diode structure in which the dimensions were adjusted so that a single diode in the center of a 1-1/4 inch wafer constituted the silicon diaphragm. This large area silicon cavity permitted a large magnification of pressure differential, and hence, resulted in a more sensitive structure. However, this structure required contacts to the diode that extended from the center of the wafer to the periphery in order that gold wires could be bonded outside the sealed cavity. Using the standard photo-resist process resulted in an unacceptably high incidence of shorts between the expanded aluminum contact on top of the oxide and the underlying silicon.

The origin of these pinholes was in the photoresistive film itself. When etching the diffused region on the ohmic contact windows, contact holes in the photoresist film permitted the oxide to be etched away from other regions as well. When an oxide hole was formed in the oxide beneath the evaporated aluminum contact path, a weak spot or a low resistance path was introduced into the structure.

Various remedies were investigated to minimize these pinholes, such as the use of resists other than the standard KPR used initially. The most common resist used in the industry at present is Kodak Metal Etch Resist (KMER). However, resolution using this relatively thick resist is sometimes marginal for the dimensions involved in the structure discussed herein. This is particularly true when defining contact holes through the existing oxide in order to establish ohmic contact to the

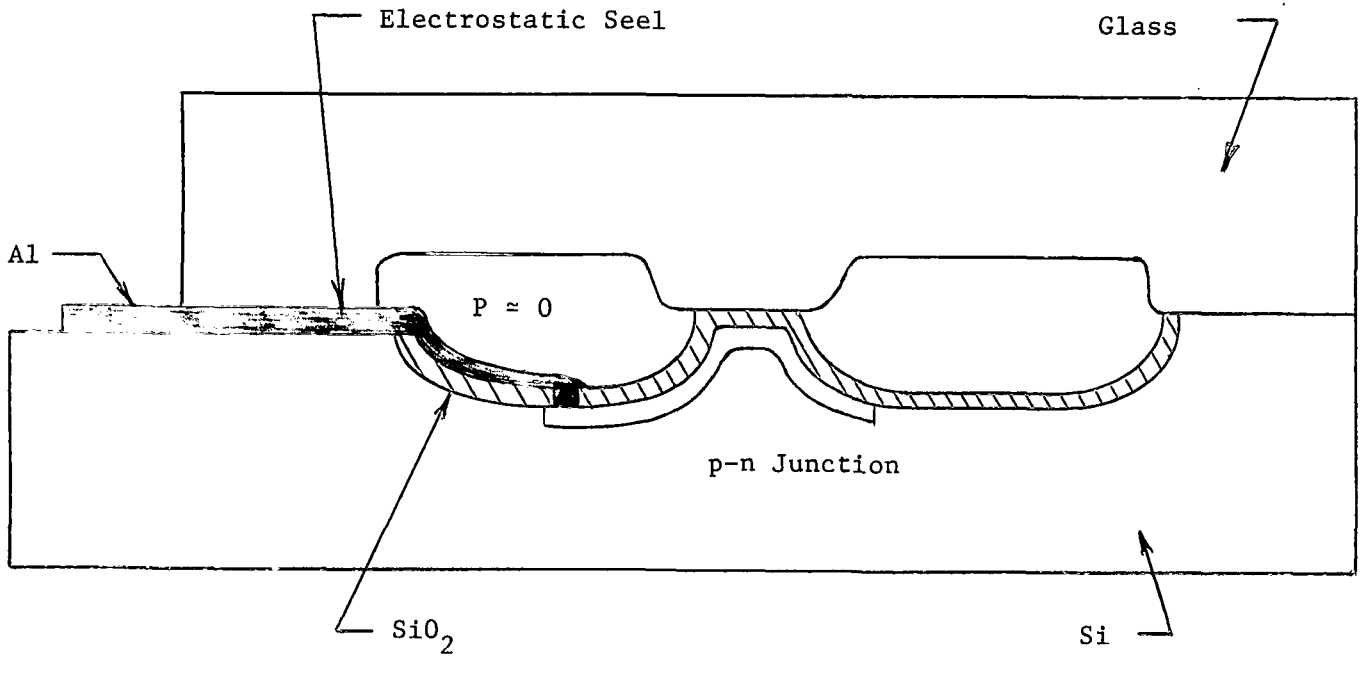


Figure 13. Initial Capsule Design

various regions of silicon. After some trial and error experimentation, the resist chosen for this project fabrication was KPR-2. This is a relatively new resist only recently developed by Kodak. It is a compromise between the highest resolution and the best etch resistance and freedom from pinholes. The resist film itself is not as thick as KMER, but it is generally thicker than the KPR utilized initially.

While the KPR-2 approach did reduce the incidence of pinholes, it did not solve the problem in a practical sense. Many devices still failed because of shorts between the connecting aluminum leads and the substrate. The practice adapted then was to employ the photoresist to define the diode regions in the center of the wafer, and to coat the bulk of the remaining wafer with black wax prior to etching. Black wax is a commercial wax dissolved in toulene or trichlorethylene and painted on the surface with a brush or other applicator. Toward the end of the fabrication program, photoresist itself was utilized in the same manner; that is, after contact printing the desired region, a thick paint-on photoresist layer was applied over the bulk of the oxide to be masked during the etch. This technique essentially solved the pinhole problem although the complete elimination of this failure mode was not achieved. This process, however, is highly unsatisfactory for a production line process and improvement is mandatory before serious manufacturing begins.

Aluminum opens at the silicon step. - A second problem that arose in fabrication was cracks in the aluminum intraconnecting contact path as it crossed over the etched diaphragm cavity boundary. This open appeared as a small, sharp crack in the aluminum film generally located at the top of the step. Two actions were taken to reduce this failure mode:

1) After standard mesa etching, the silicon wafer was given a short post etch with no mask in place in order to further round any corners existing as a result of the silicon etch. If the total etching time to form the desired mesa height was 60 seconds with the oxide mask in place, for example, the oxide was removed and the silicon wafer reimmersed in the silicon etch with no mask at all for another 8 seconds. During this post-etch, the sharp corners existing at the cavity edge were attacked more rapidly and hence tended to be rounded and present a less abrupt change in topography for supporting the aluminum film.

2) In the vicinity of the boundary between the etched cavity and the outer ledge, the aluminum stripe was covered with additional etch masking material after photoengraving but prior to etching. This additional masking was on the aluminum stripes only. Because of the step in the surface the thickness of the spun-on photoresist is less uniform and generally results in a thinner than normal coating at the

top of the step--the location at which cracks in the aluminum were observed to appear. The additional masking material prevented aluminum removal at the step during etching. These two actions significantly reduced aluminum strip failures.

Large surface components in the diode current-voltage characteristics. The most serious shortcoming in the diodes fabricated was large surface components of current in the current-voltage characteristic of the diodes. The source of these large surface components was never fully traced, but is presumed to be primarily a reflection of contamination during various processing steps, although the mask design probably contributed to the problem. Surface current components manifest themselves as non-ideal currents, particularly at low values of forward bias. They are readily recognizable on plots of log-current versus voltage (log I-V) as departures from the ideal $\frac{q}{kT}$ slope. Bulk generation-recombination components also contribute to departures from ideal behavior, but these components exhibit $\frac{q}{2kT}$ characteristics. Surface components, particularly channels, are characterized by a log current dependence of $\frac{q}{nkT}$ where n is greater than 2. The diodes fabricated exhibited both dependences and while the existence of a value of n> ' virtually guarantees that the diodes is dominated by its surface properties, the converse is not true. Low bias behavior of $\frac{q}{2kT}$ does not guarantee that the source of the non-ideal current is bulk regeneration-recombination. Surface current components can also exhibit this voltage dependence.

Other evidence suggesting that the surface was dominating the electrical characteristics of the diodes fabricated was their susceptibility to relatively mild heat cycles in various ambients (such as that associated with the electrostatic sealing process, or with the sintering operation used to reduce the series resistance of ohmic contacts). These relatively low temperature processes modified the properties of the junction dramatically, strongly suggesting that the modifications seen are those due to surface components.

To eliminate surface components requires clean processing conditions. Contamination can be introduced from mishandling prior to receiving wafers, during any of the processing steps such as oxidation, diffusion and metallization or from handling during testing. One of the most successful methods for evaluating the cleanliness of a process is to grow an oxide in a given furnace and then subject MOS capacitors fabricated from the oxide to various bias-temperature stresses. A state-of-the-art, clean oxide can withstand 300°C under a field of 5×10^5 V/cm to 10^6 V/cm without exhibiting any noticeable change in its capacitance-voltage characteristic. Such tests carried out in the RTI laboratory have consistently revealed oxides inferior to the state-of-the-art.

A second cause of extraordinarily large surface components arises in the design of the capsule diode. In this design, the diffused area is narrower than the oxide mask used to etch the mesa. This disparity in relative sizes means that the junction intersects the surface of the silicon partway up the mesa side. This circumstance itself is not obviously objectionable, except that experience in printing the various photomasks using planar-mesa substrates shows that light reflection from the mesa walls during exposure causes non-uniformities in the regions printed. Consequently, the periphery of the diffused region is not the rectangular region designed into the masks, but a distorted cloverleaf geometry of extra long periphery such as illustrated in Fig. 14. This type of pattern greatly increases the surface component of current because of the increased periphery of the junction. In addition, the fact that the junction occurs well up the side of the mesa means that some of the stress loading the mesa also appears in this region. Consequently, any stress sensitivity of the surface component is reflected in the diode stress sensitivity characteristic. Surface components are notoriously uncontrollable and, in general, units exhibiting a large component of surface current were not processed further so that little stress testing of these surface components was carried out.

Correction of these two deficiencies--the one in processing cleanliness and contamination control; the other in mask design--are two recommended steps for improving the diode characteristics. Neither of these steps were taken during this program. In any continuing activity, modifications in procedures to eliminate both sources of surface currents should be a first order of priority.

Both p-on-n and n-on-p structures were investigated throughout the course of the program in an effort to improve the quality of the resulting diodes. Results were comparable with the two processes with the exception that yields were higher on using a p-type substrate with an n-diffusion. Additionally, this configuration, in principle, can be a one-diffusion process since the aluminum used to establish ohmic contact to the diffused region can also be used to establish ohmic contact to the substrate. When using the reverse configuration, an additional n+ diffusion must be carried out in order to create a region of n-type impurity sufficiently heavily doped so as to avoid forming a p-n junction when the aluminum is alloyed into the silicon.

The final procedures utilized in fabricating the diodes are described in Appendix B, and a detailed description of the mask-set is included in Appendix A.

Summary

The major fabrication problem was an inability to eliminate surface components from the diode I-V characteristics. State-of-the-art fabrication

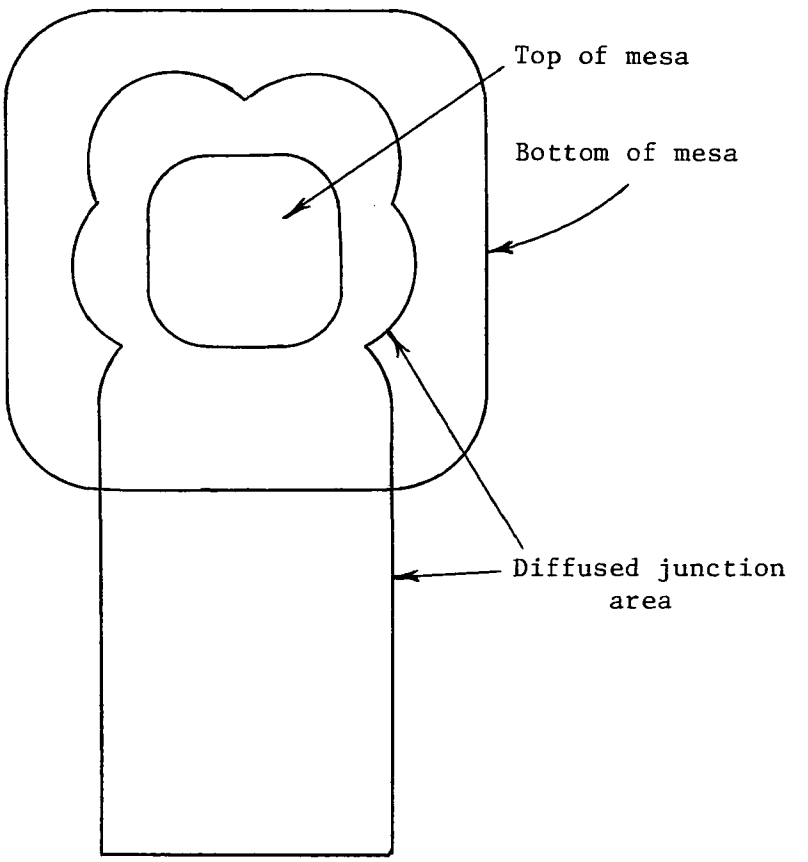


Figure 14. Uneven Etch of Junction Area Close to Top of Mesa.

can reasonably expect a two order-of-magnitude improvement over what was routinely observed at RTI. Other diode design features seemed adequate.

The present diode design is not necessarily optimum, but shortcomings in design are overshadowed by fabrication problems at present.

SECTION V

TRANSDUCER FABRICATION

The Capsule Diode

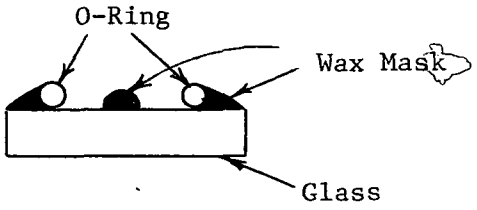
Component Fabrication. - A sketch of the capsule diode is shown in Fig. 8. The dimensions included correspond to a 2 × 2 array of diodes on a single wafer. The diameter of the cavity etched in the silicon is 266 mils, and the cavity depth is approximately 3 mils. The processing steps for fabricating the planar-mesa diodes are described in Appendix B. Appendix A includes additional detail with a description of mask sets for both 2 × 2 and 3 × 3 diode arrays on a single water.

The port-side and vacuum-side glass wafers in Fig. 8 are a heat resistant, drawn glass. Cavities are formed in the glass wafers by etching in an agitated 50% HF solution. This process is illustrated in Fig. 15, The wafer thickness is fixed by mechanically lapping the backside and the corners are removed by grinding against a silicon-carbide surface. Finally, the center post is lapped with a 3 μ alumina compound as a precaution against sealing between the planar-mesa diode and opposing glass pressure-post during the anodic bonding procedure. The vacuum-side glass wafer is formed in a similar fashion; however, only a single etch-step is required for this less-complex structure. An illustration of the completed port-side and vacuum-side glass wafers is shown in Fig. 16.

The final component of the capsule diode is the silicon diaphragm containing an array of planar-mesa diodes. Semiconductor processing procedures for fabricating these diodes are described in Appendix B. Additional steps are as follows: (1) the 0.008" wafer is lapped, etched and mechanically polished on the back surface to yield a 0.004" diaphragm with a polished surface suitable for anodic bonding, (2) the wafer is scribed to separate the various diodes, and (3) masked with black wax and etched to yield the desired shape. One mil (.001") gold leads are T.C. bonded to complete the structure.

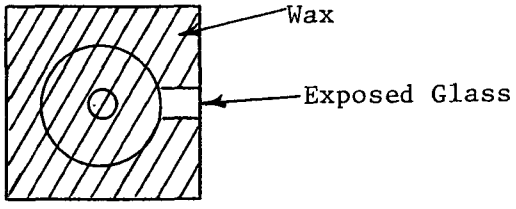
Component Assembly.- The assembly of the glass wafers and planar-mesa diodes into capsule diodes utilizes the anodic bonding procedure described by Pomerantz and others at Mallary (ref. 10). The initial step is to bond the vacuum-side wafer to the back of the silicon diaphragm in a vacuum so as to form a vacuum-reference cavity. Figure 17 illustrates this procedure. The quartz plate provides a means of applying the 300 g force at the silicon-glass interface, but does not take part in the bonding procedure. The anodic bonding occurs only between the silicon diaphragm and glass wafer. The dc current is initially constant at approximately 200μA until bonding occurs. After the bond forms, current decreases significantly. The heater circuit and dc circuit are then opened and the assembly allowed to return to room temperature.

The port-side wafer is sealed to the silicon diaphragm in a similar process, but at an atmosphere of pressure. This apparatus is illustrated in Fig. 18. This seal completes the capsule diode structure illustrated in Fig. 8.

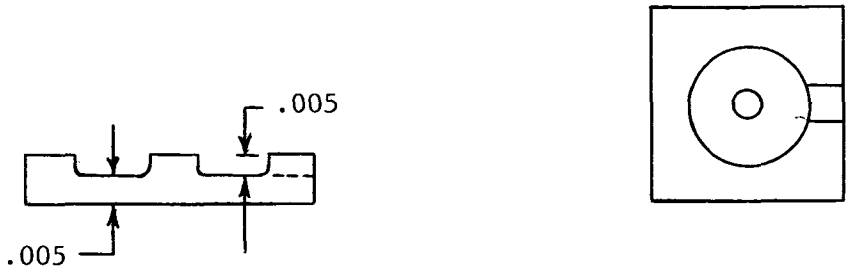


(a) Masking Technique for 1st Etch

(b) Port-side Glass Wafer after 1st Etch

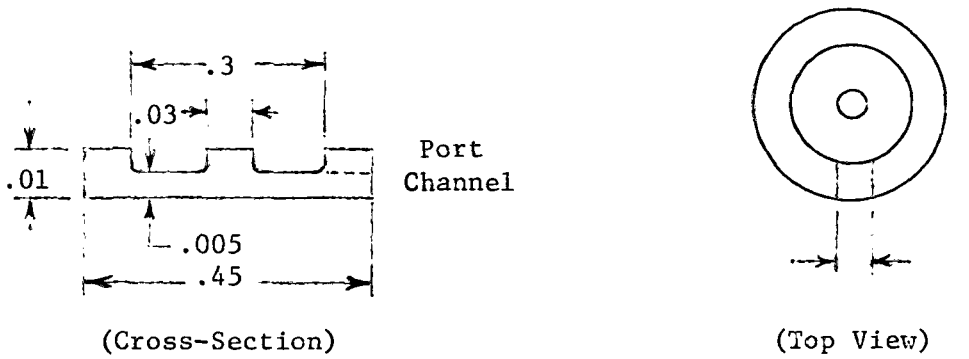


(c) Masking for 2nd Etch (Pressure Port)

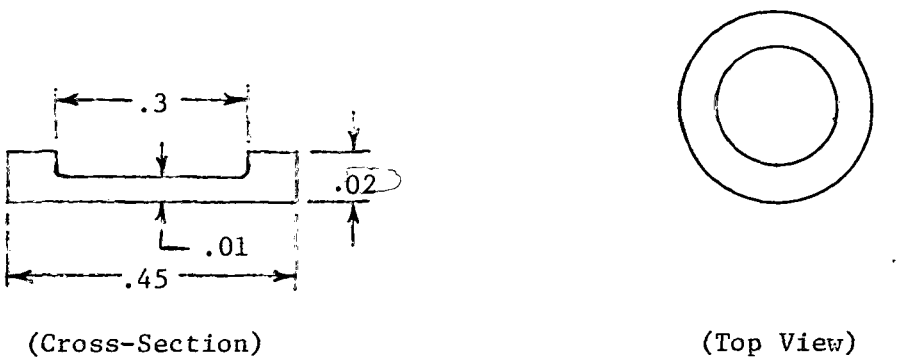


(d) Port-side Glass Wafer after 2nd Etch

Figure 15. An Illustration of the Glass Wafer Fabrication Technique (all dimensions in inches)



(a) Port-side Glass Wafer



(b) Vacuum-side Glass Wafer

Figure 16. An Illustration of the Completed Port-side and Vacuum-side Glass Wafer

(all dimensions in inches)

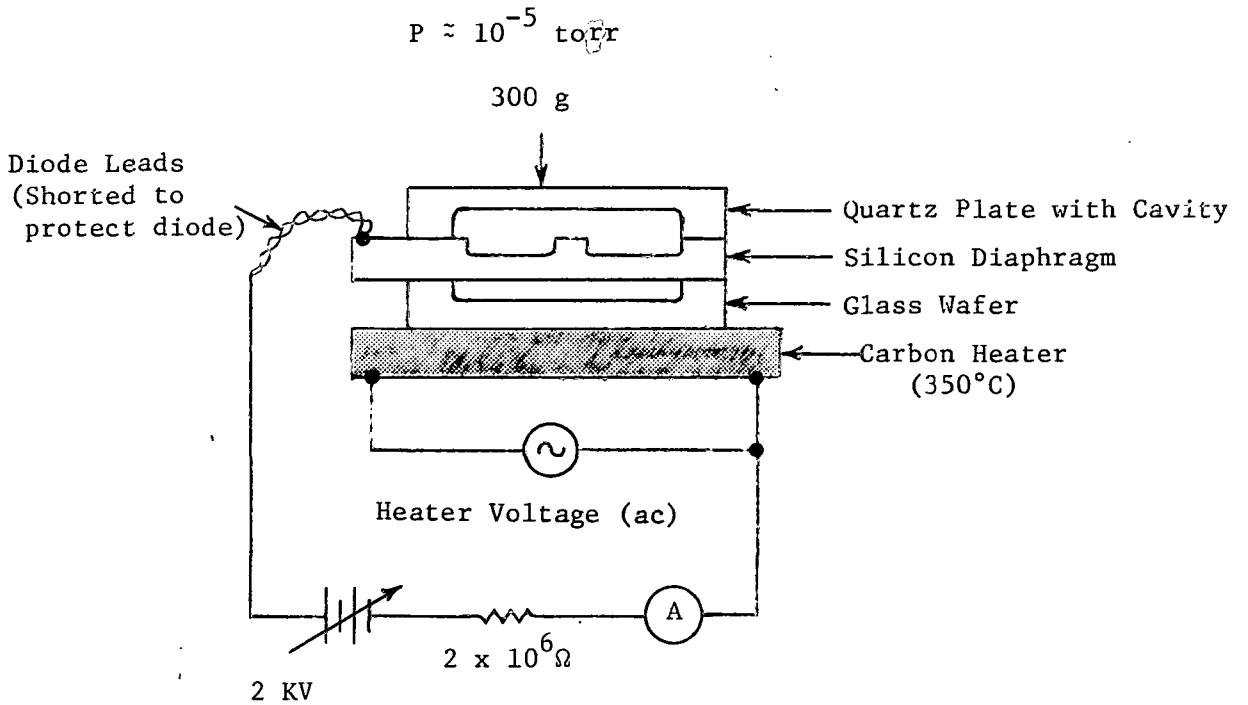


Figure 17. An Illustration of the Anodic Bonding Procedure.

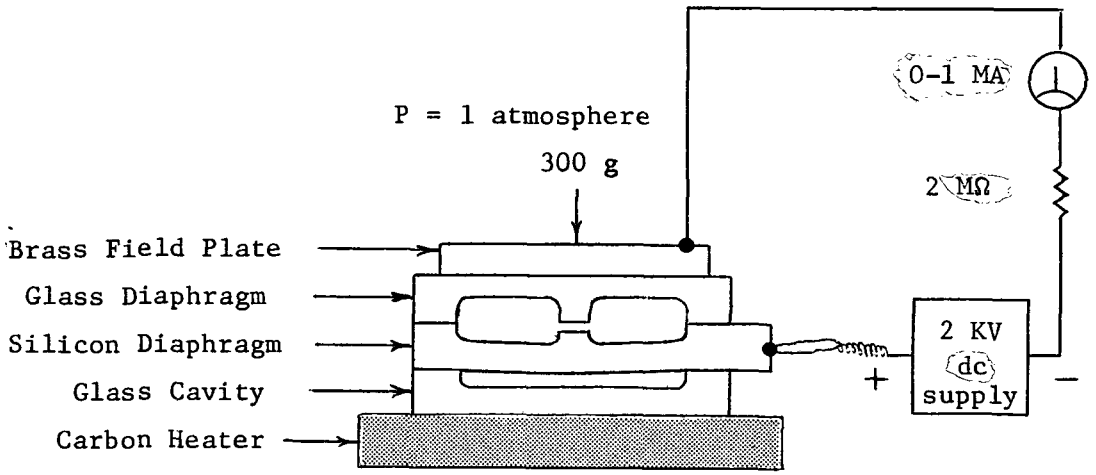


Figure 18. Anodic Bonding Apparatus for the Port-Side Cover.

A photograph of the completed capsule diode is included in Fig. 19.

Transducer Housing

In Fig. 20, the capsule diode is shown mounted in a housing that completes the transducer. The two piece, ceramic housing is bonded together with epoxy to securely hold the capsule diode around its perimeter as illustrated. It provides complete protection for the capsule diode, and contains a bias spring and bias adjust screw for setting an initial stress-bias on the transducer. The housing material is a commercially available ceramic that can be conventionally machined into precision parts. After machining, the ceramic material is hardened by firing in an oven.

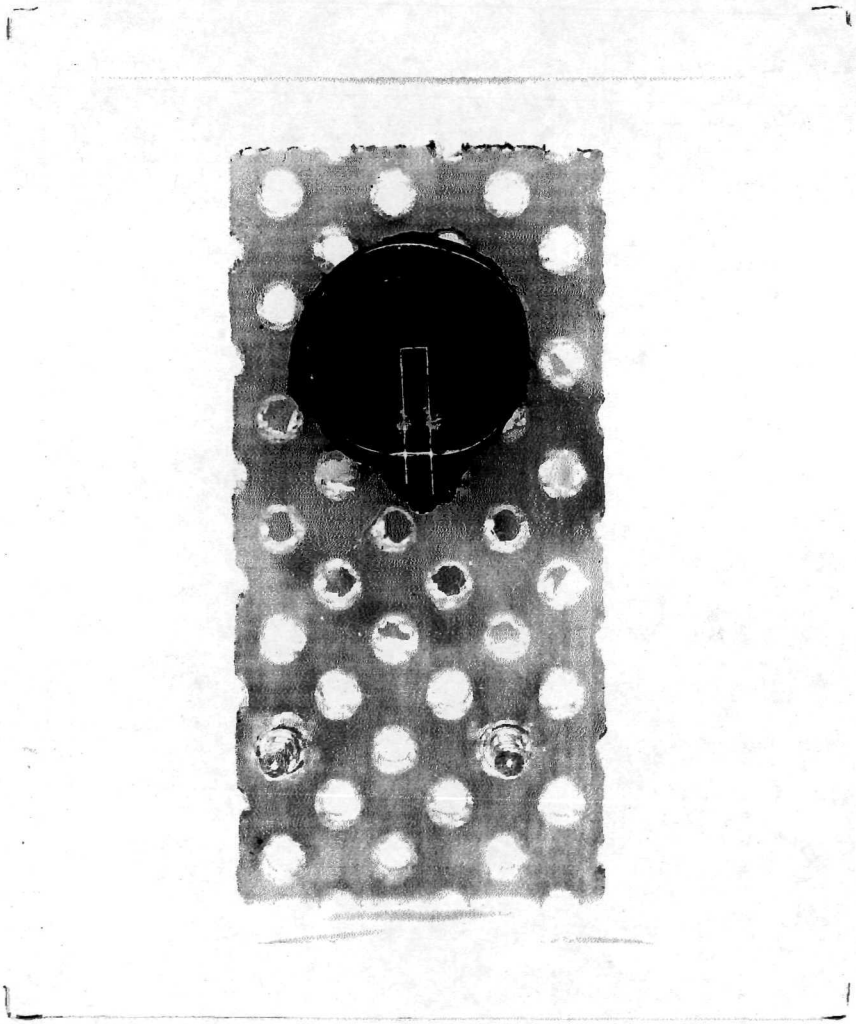
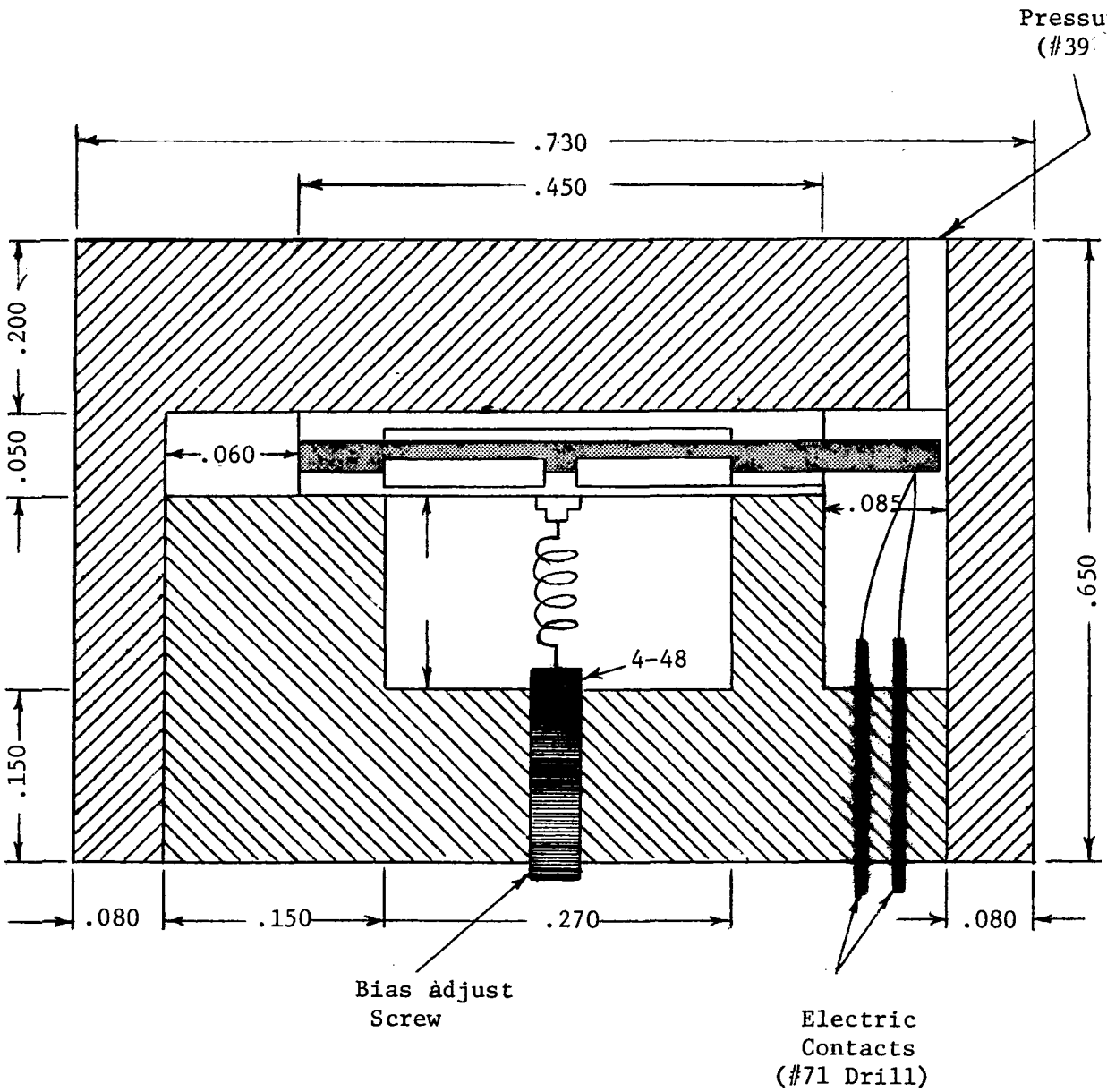


Figure 19. Photograph of a Completed Capsule Diode



(all dimensions in inches)

Figure 20. An Illustration of the Complete Transducer.

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SECTION VI

EXPERIMENTAL RESULTS

Introduction

Diodes suitable for use as a piezojunction sensor have been discussed previously in this report. Some diode characteristics e.g., junction depths and surface carrier concentrations, are measured destructively for a given set of diffusion parameters and remain relatively unchanged. Physical geometries are fixed by the mask-set and, in the case of the planar mesa diode, the etching parameters. Other controlling parameters are the resistivity and orientation of the starting silicon. Every effort was made to optimize these various parameters. After the diodes were processed, their quality was judged on the basis of their easily observed I-V characteristics.

The ideal diode has been previously described. In summary, it is a diode whose log current versus voltage (log I-V) plot has a constant slope of q/kT extending over several orders-of-magnitude change in current (I). This ideal curve is included in Fig. 21 along with the curve of a good quality diode used as a standard during later stages of this investigation. The standard curve in Fig. 21 was frequently used for comparison purposes and is found on many of the diode and transducer curves included in this report.

The standard diode in Fig. 21 illustrates some of the limitations that are encountered in practical diodes. Its slope, while significantly better than the q/2kT indicative of generation-recombination currents, is clearly not the ideal q/kT. The slope decreases in the vicinity of 0.3 V as predicted by the diode equation. At higher current levels, e.g., current levels corresponding to greater than 0.7 V bias, the slope again decreases due to the presence of spreading (series) resistance in the silicon.

The standard diode, log I-V plot shown in Fig. 21 was generated in a log current plotter circuit. This plotter was used to generate most of the log I-V plots in this report. Its validity was established by comparing the standard diode curve with a point by point plot, and checked frequently by comparing the standard with this original data. The circuitry for this plotter is shown in Fig. 22 where the D_m is the diode to be measured.

Discussion

Numerous silicon wafers were started through processing to become planar mesa diodes, capsule diodes, and finally pressure transducers. The yield of transducers was low. Most of the starting

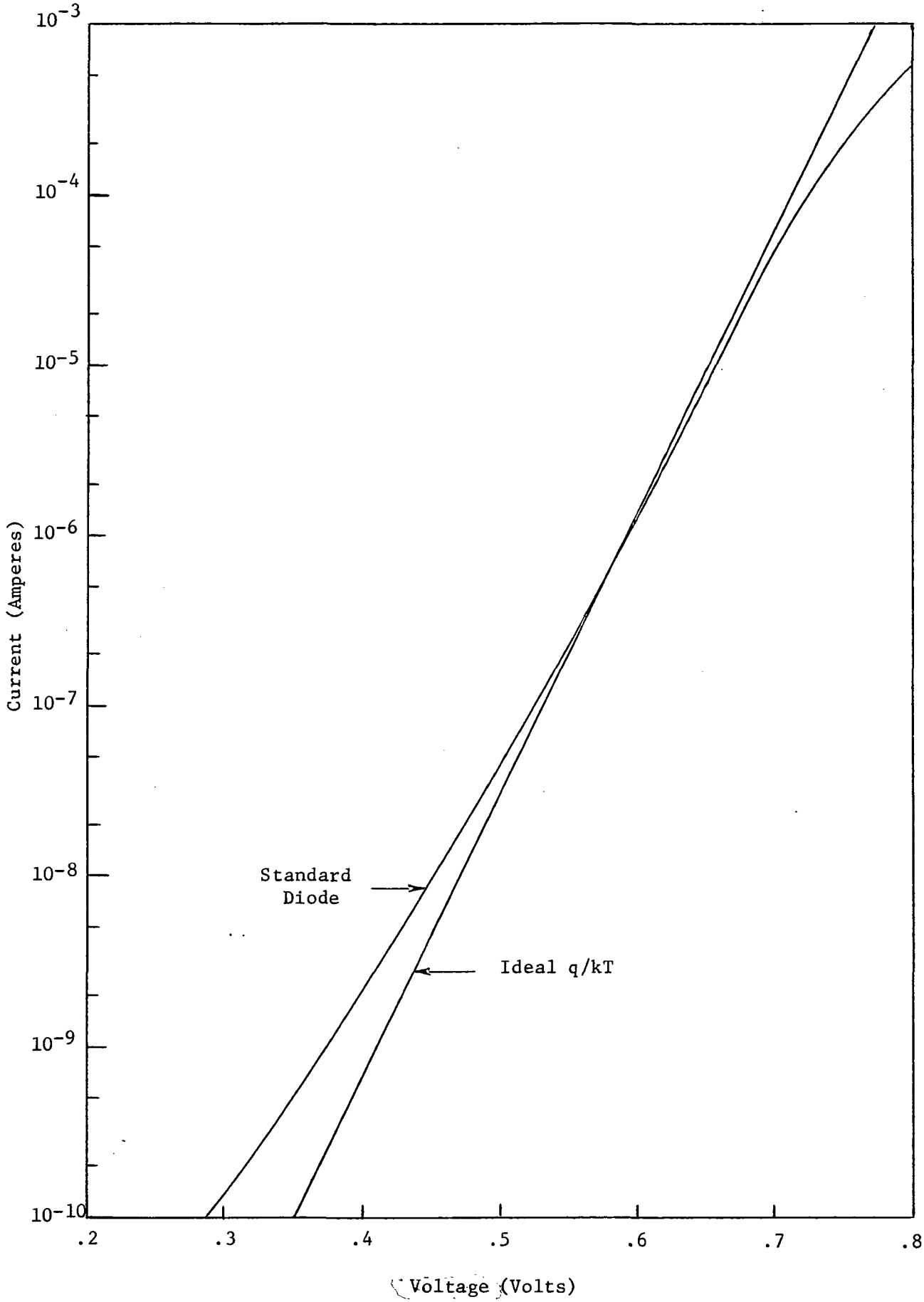


Figure 21. Log I-V Characteristics of the Standard Diode and the Ideal q/kT Slope.

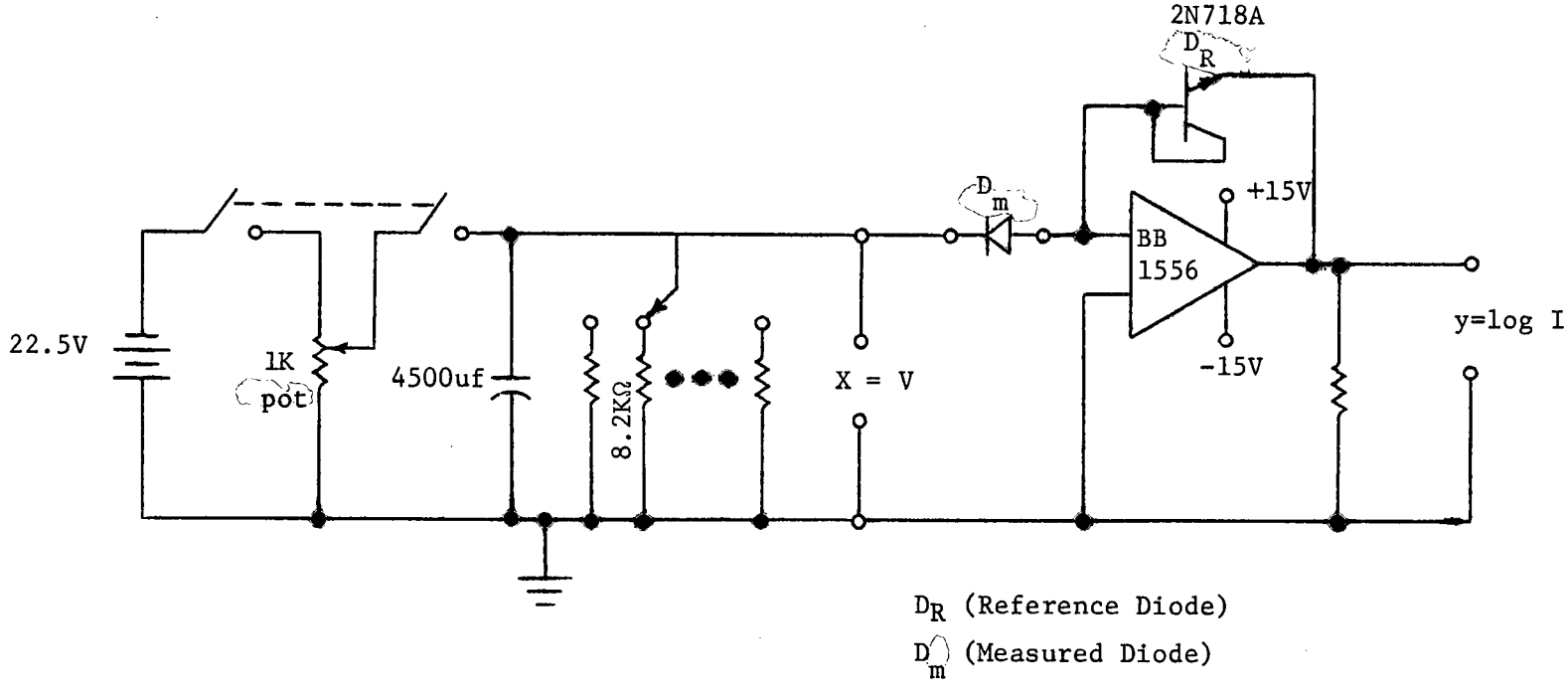


Figure 22. Log Current Versus Voltage Plotter Circuit

wafers were dropped after semiconductor processing, and others were lost during sealing operations. This section discusses the characteristics of some of the units that eventually yielded transducers.

Some earlier planar-mesa diodes. - Some of the best slopes, i.e., approximately q/kT, were achieved early in the program as illustrated in Fig. 23. In Fig. 23, the log I-V characteristics of two planar-mesa diodes are compared with an ideal q/kT slope. At current levels below 10 μA, these diodes were nearly ideal, but the series resistance effect is apparent above that current level. (Data points were not taken below 10^{-8} A.) These earlier diodes were not compatible with the capsule diode design. The mask-set provided for one diode per wafer, and the etched diaphragm area was too large for the capsule concept.

The curves of Fig. 23 were generated from point by point data, but they are presented on the standard scale used throughout this report to enhance comparisons.

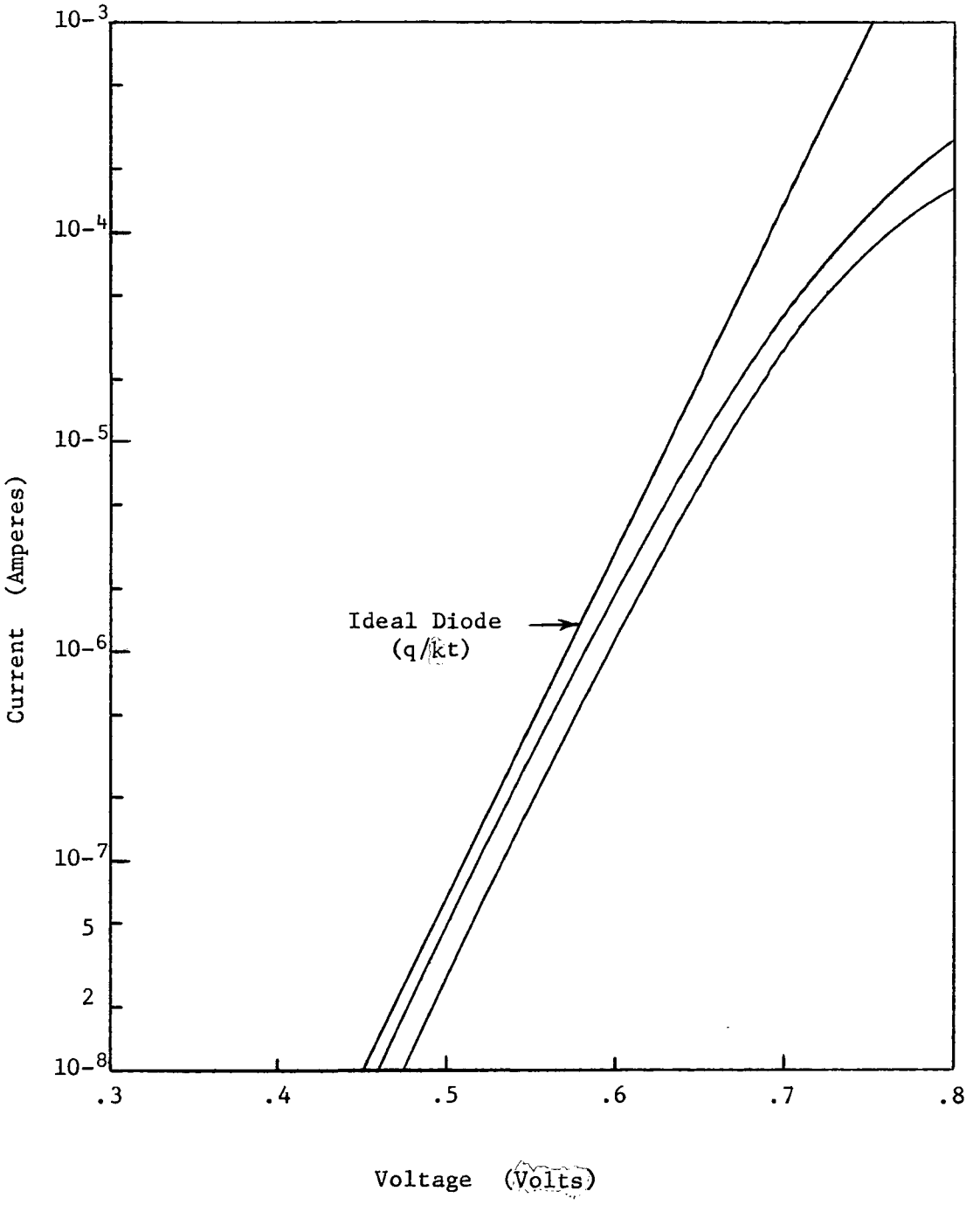


Figure 23. Log I-V Characteristics of Large Area, Planar-Mesa Diodes

Transducer No. 1

The log I-V characteristics of the diode used in Transducer No. 1 are illustrated in Fig. 24. These curves suggest that the diode had surface leakage problems that were influenced by moderate heat during additional processing. Although the final curve, i.e., the capsule diode curve, compares closely with the standard diode, the initially poor characteristics caused concern over the long-term stability of the diode.

The planar-mesa diode curve in Fig. 24 suggests the diode is unusable. It is a poor diode with only a narrow region of acceptable slope. Series resistance is apparent above 0.7 V, and surface leakage is in evidence below that value. The steep slope at very low voltage biases is unexplained. After the vacuum-side seal was completed, the diode was even more dominated by surface problems. When completed as a capsule diode, the characteristics are greatly improved. Apparently, the heat applied during the sealing operation has altered the surface properties.

As a completed, housed transducer, the characteristics of a unit are partially determined by the stress bias, i.e., the force applied by the bias spring of Fig. 20. The log I-V characteristics of Transducer No. 1 are illustrated in Figs. 25 through 28 for various bias conditions. The bias was set in each case with the transducer in a vacuum since this also set the maximum stress the capsule diode would experience (increasing the pressure reduced the applied stress.) The 50 μmHg curve in each figure corresponds to the initial bias. The limiting effect of the series resistance is readily apparent in each figure. In Fig. 25, for example, the series resistance limits the usefulness of the transducer to a voltage bias below 0.6 V. Generally it is advantageous to operate at a high voltage bias.

By altering the initial stress bias, the region of sensitivity for the transducer can be changed. In Fig. 25, for example, the initial stress bias was such that at 300 mm Hg, the stress was removed and the transducer was insensitive to further pressure increases. In Fig. 26, the initial stress bias was significantly higher and relatively large changes occurred between 300 mm Hg and in 700 mm Hg.

None of the transducers described in this report were significantly stress-biased with the biasing spring. So few were completed that it was decided not to risk damaging them by applying a higher stress. In each case, significant increases in sensitivity could have been gained with increased stress.

Fig. 27 illustrates a third initial stress-bias condition, and Fig. 28 a fourth. Additionally Fig. 28 illustrates the lack of repeatability achieved in this transducer. (The three lines labeled with resistance values in Fig. 28 are discussed in a subsequent section on instrumentation). The initial bias was set at a pressure of 50 μHg and several curves plotted

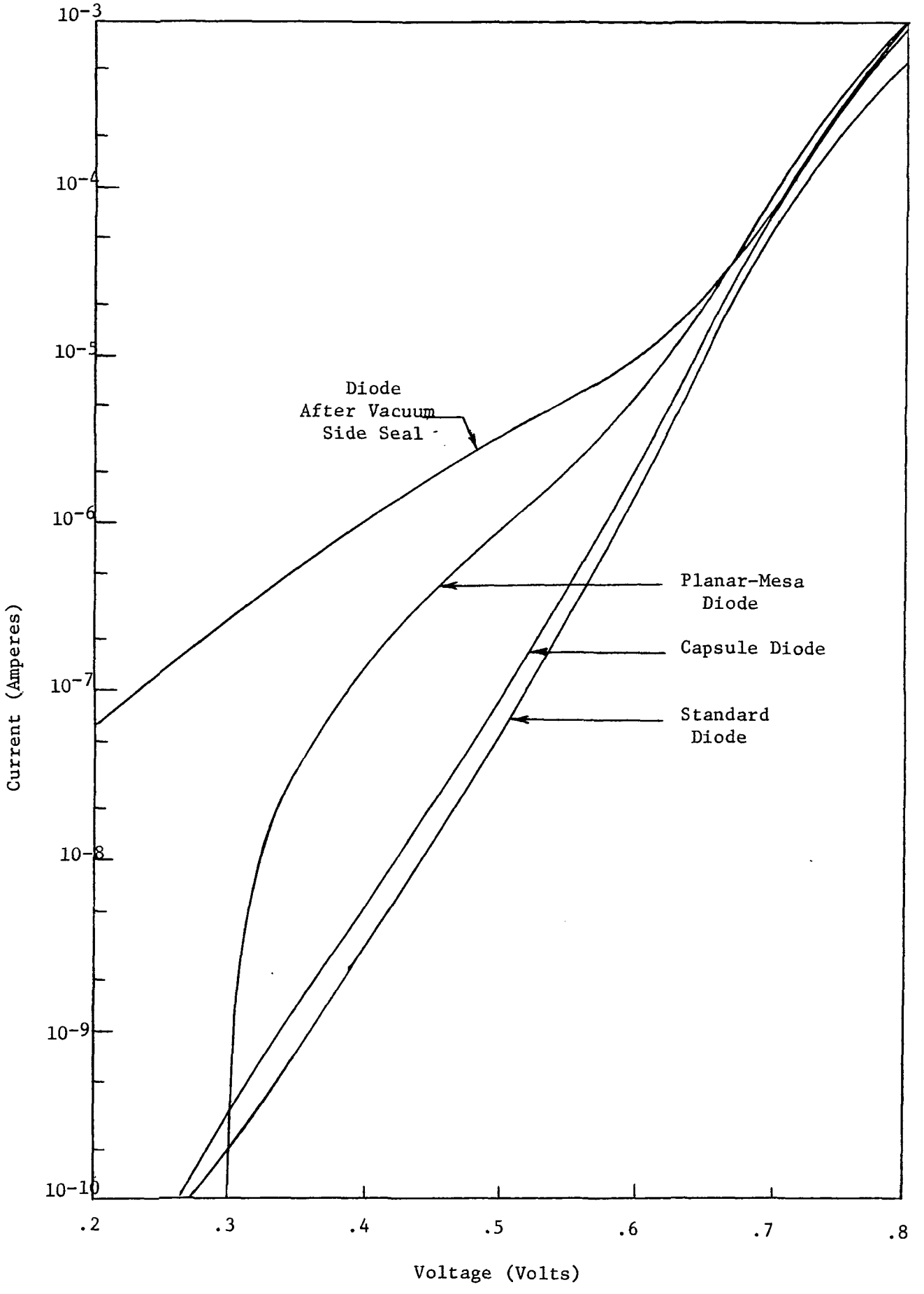


Figure 24. Log I-V Characteristics of Transducer No. 1 Diode at Various Stages

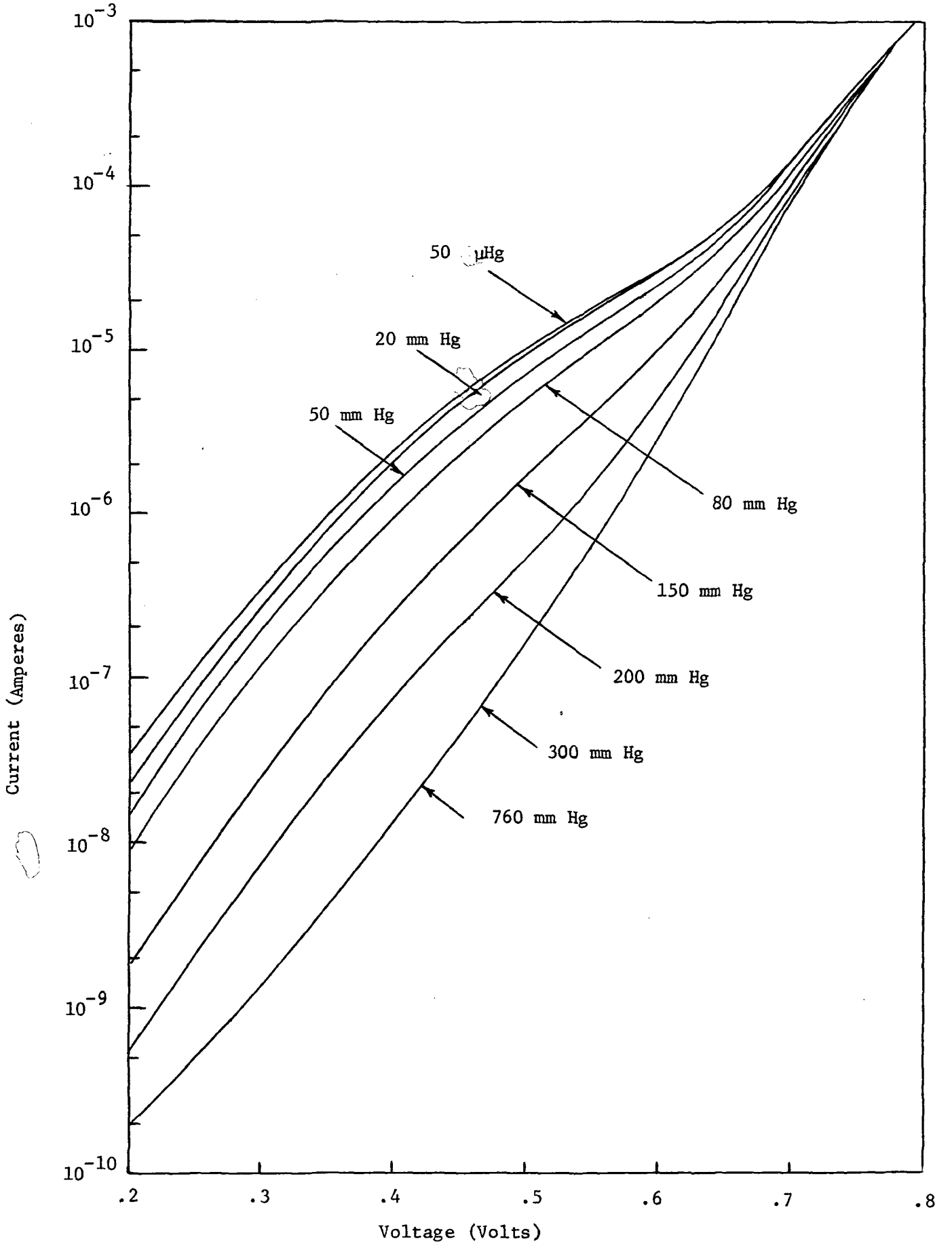


Figure 25. Characteristics of Transducer No. 1; Bias Condition 1.

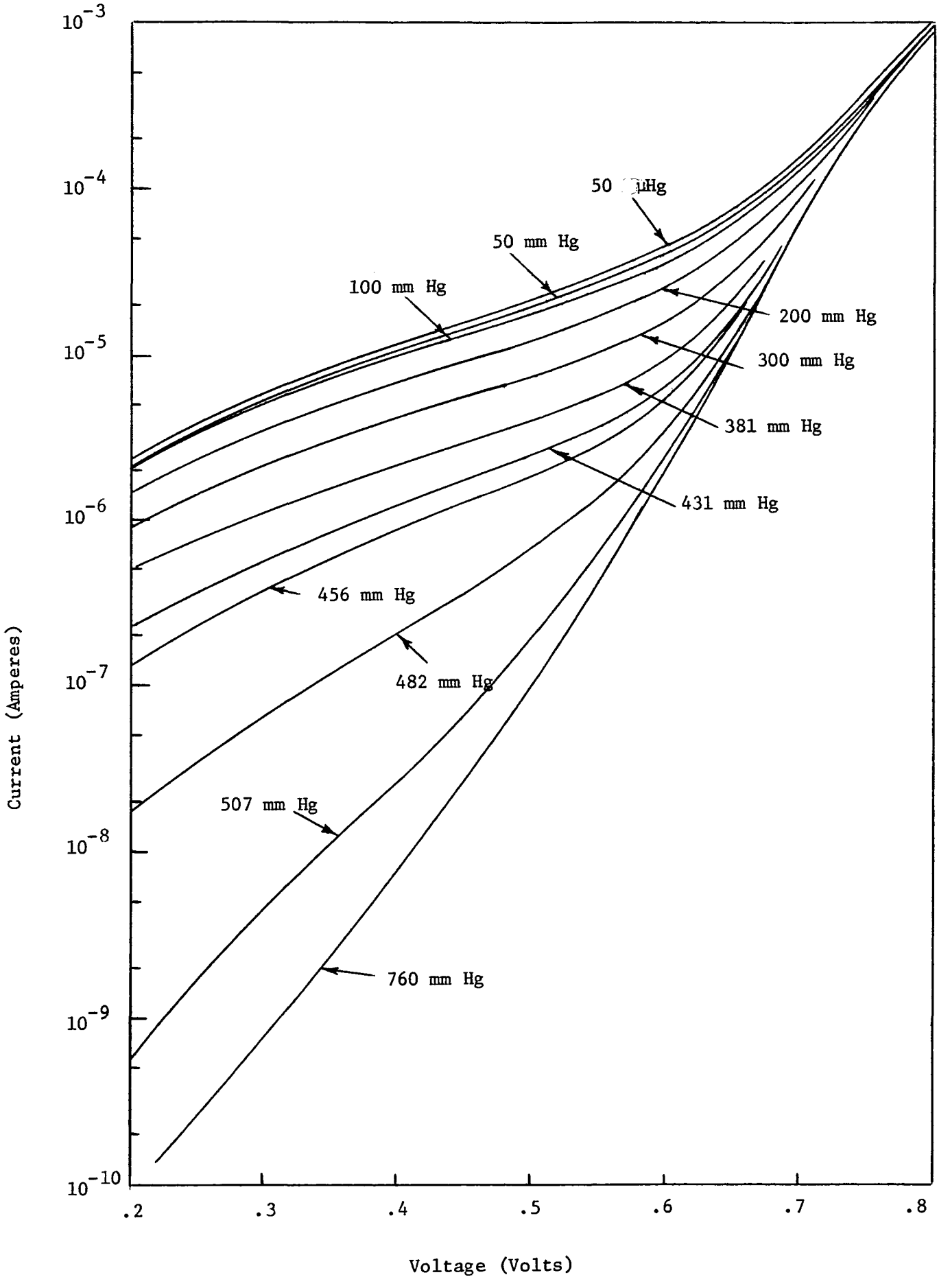


Figure 26. Log I-V Characteristics of Transducer No. 1; Bias Condition 2.

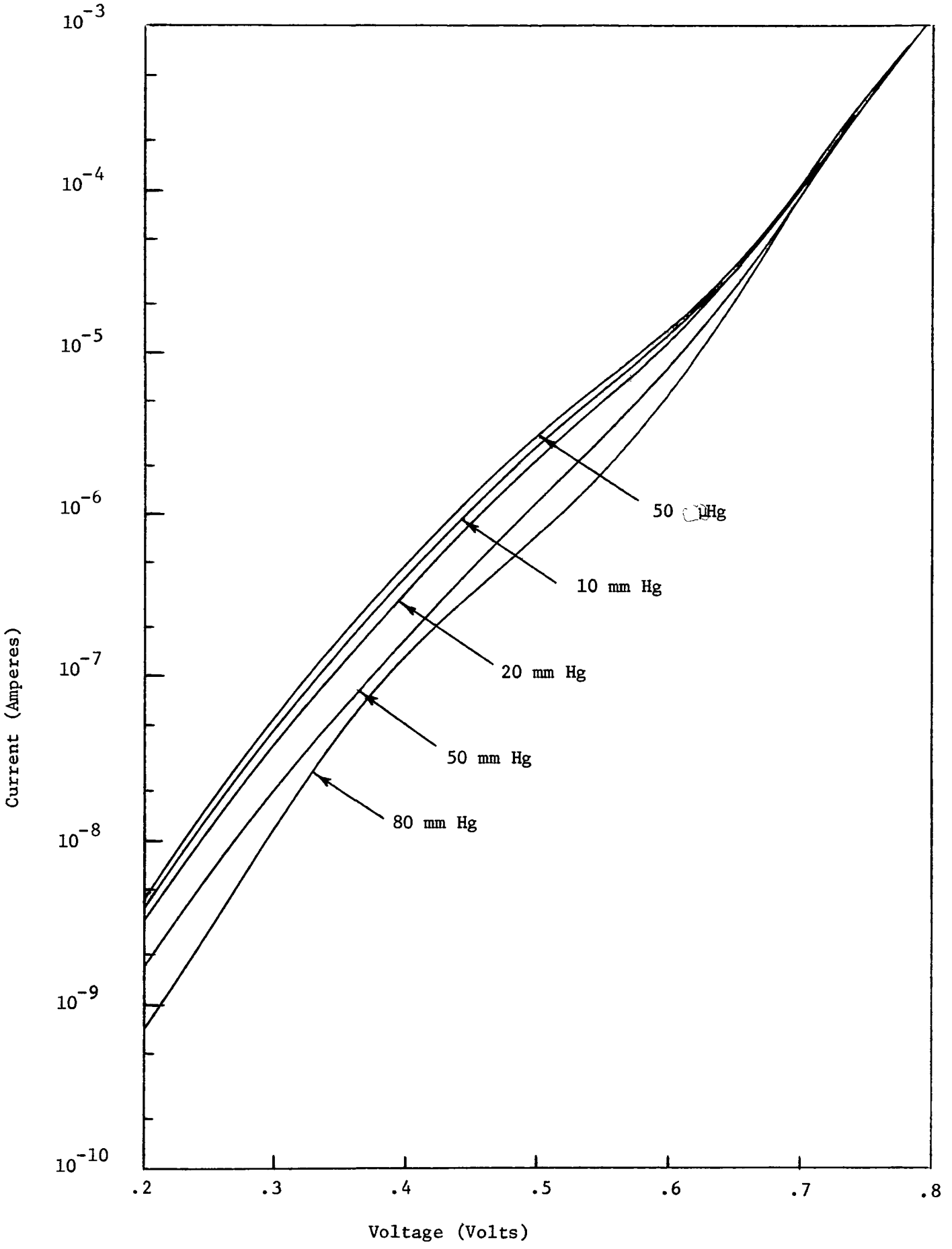


Figure 27. Log I-V Characteristics of Transducer No. 1; Bias Condition 3.

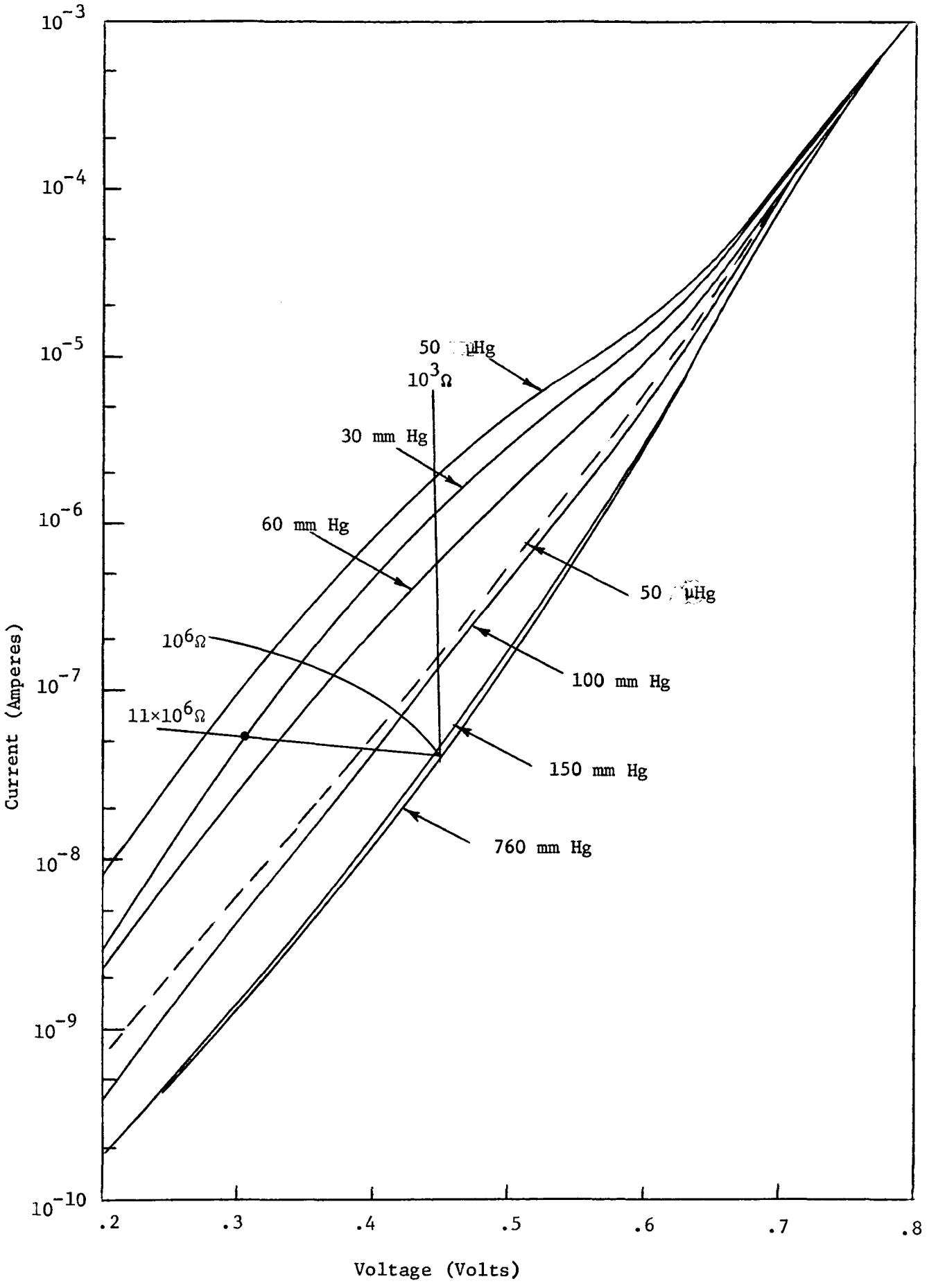


Figure 28. Log I-V Characteristics of Transducer No. 1; Bias Condition 4

corresponding to pressure increases to 760 mm Hg. The pressure was decreased again to 50 μHg and the plotter circuit operated. The results are shown as a broken curve in Figure 28. This lack of repeatability is traceable to the housing. When unhoused diodes were subjected to ON-OFF stress conditions, the results were repeatable.

Transducer No. 2

The log I-V characteristics of the diode used in fabricating Transducer No. 2 are shown in Fig. 29. This diode shows the characteristic resistance effect above 0.7 V, and some surface leakage. It is reasonably a good diode, however. The minimum slope is significantly greater than the q/2kT characteristic of generation-recombination current. During the sealing process, this diode was also improved to have the characteristics shown in Fig. 30. The 200 mm Hg curve in Fig. 30 corresponds to the capsule diode without any stress-bias. This transducer was stressed-bias in a vacuum (50 μHg curve) and the curves of Fig. 30 generated. All of these curves compare favorably with the q/kT slope, and the transducer appeared very stable. When the pressure was returned to 50 μHg, the original curve was retraced.

Fig. 31 is a similar set of curves for a slightly different bias condition. The 50 μHg curve was again retraced.

The curves of Figs. 30 and 31 indicate that Transducer No. 2 is most sensitive for a voltage bias of 0.55 volts. Consequently, a constant voltage bias of 0.55 volts was arranged, and the current recorded as pressure was increased from 1 mmHg to 200 mmHg and returned. These data points were immediately repeated, and the results are shown in Fig. 32. The hysteresis is thought to be a result of the capsule design as discussed in Section III.

Transducer No. 2 failed before additional test could be run when an aluminum stripe open circuited the diode. This failure mode was also observed in other transducers.

Transducer No. 3

The curves in Fig. 33 include the diode used in Transducer No. 3, the diode after the vacuum-side seal was completed, the capsule diode curve, and the standard for comparison purposes. Although the completed capsule diode compared favorably with the standard, the significant changes that occurred during fabrication of the capsule diode suggests surface problems.

Figs. 34, 35, and 36 show the log I-V characteristics of Transducer No. 3 for three different initial stress-bias conditions. As before, the 50 μHg curve corresponds to the maximum stress

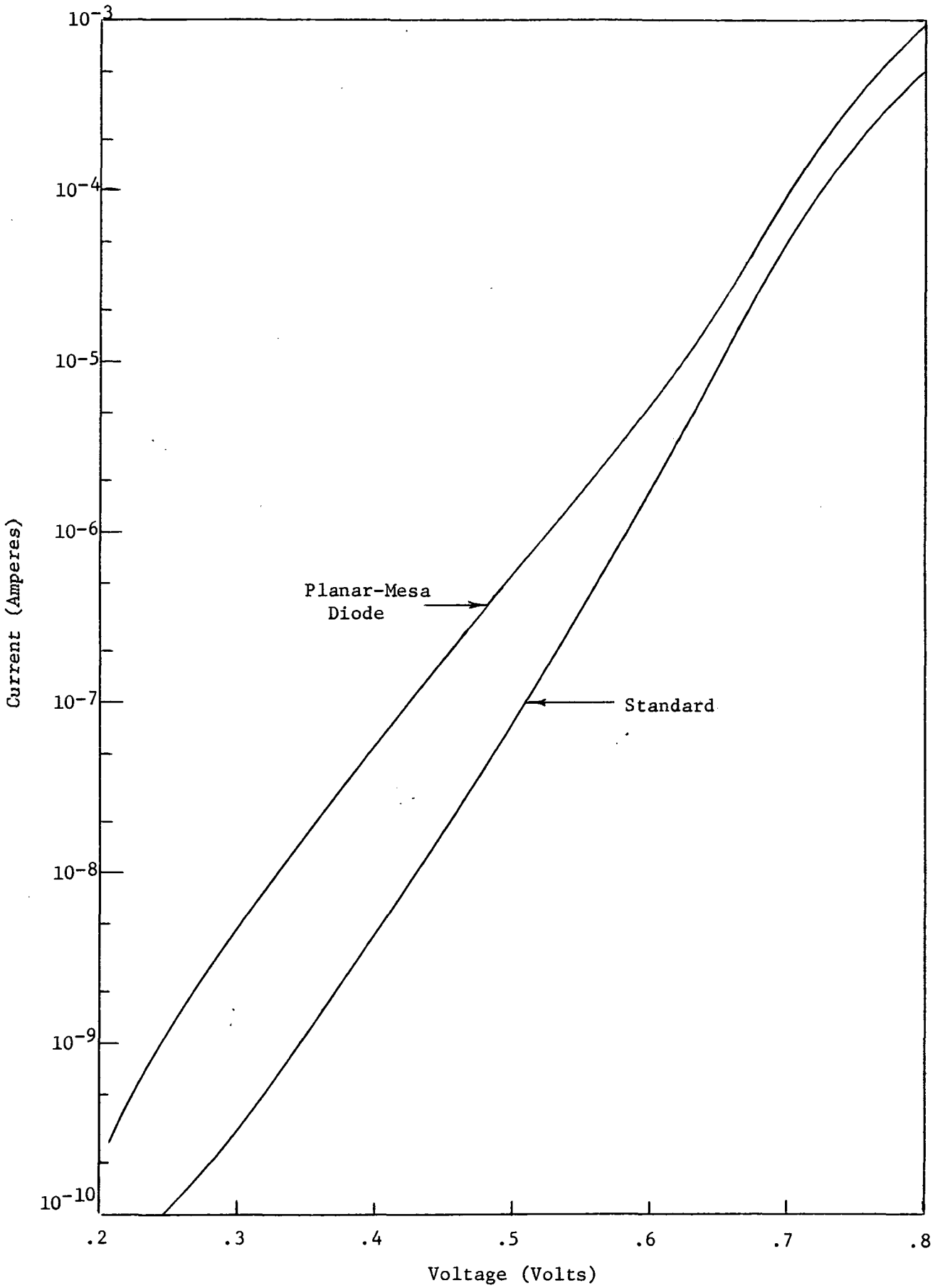


Figure 29. Characteristics of the Planar-Mesa Diode. Used in Transducer No. 2

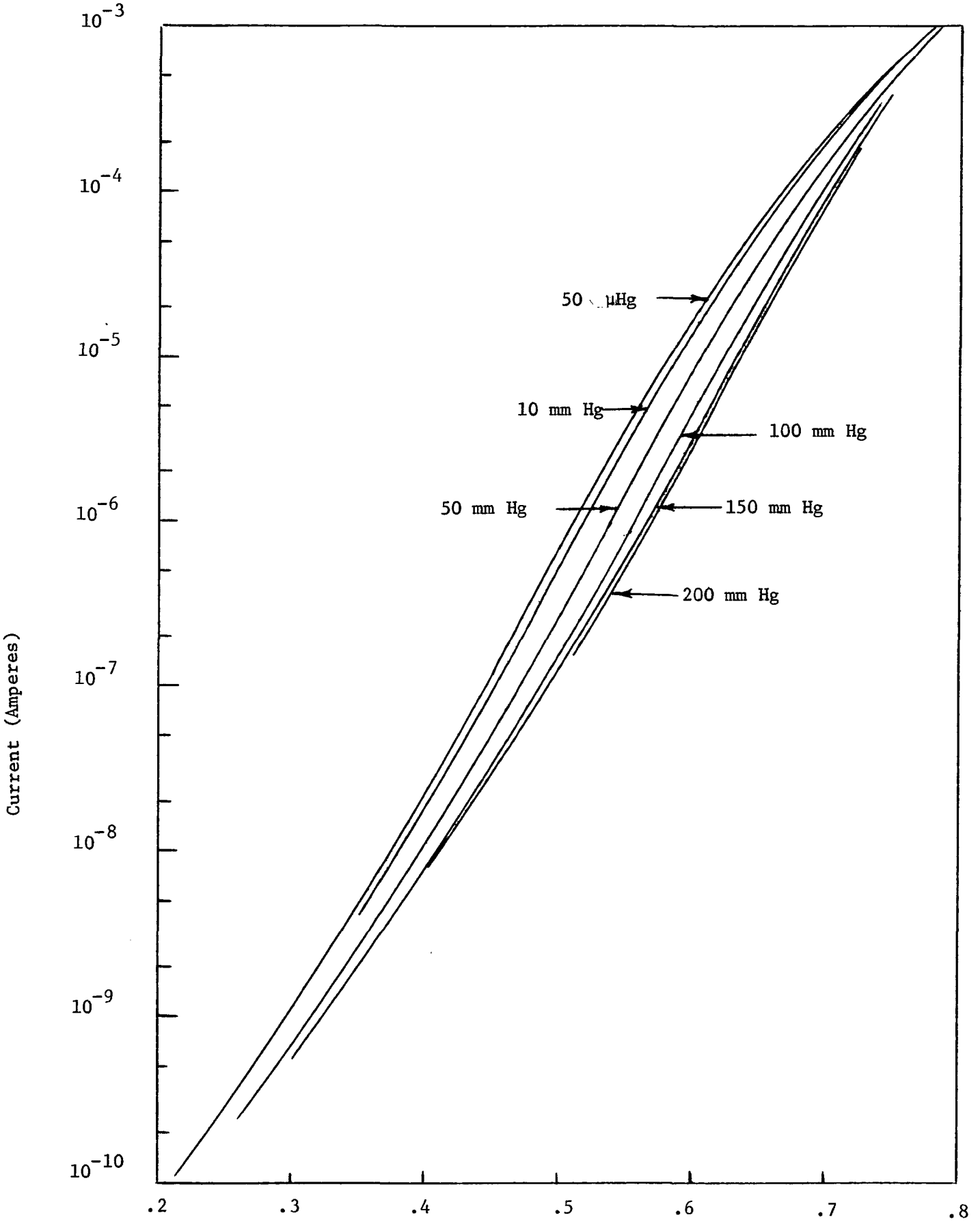


Figure 30. Log I-V Characteristics of Transducer No. 2; Bias Condition 1.

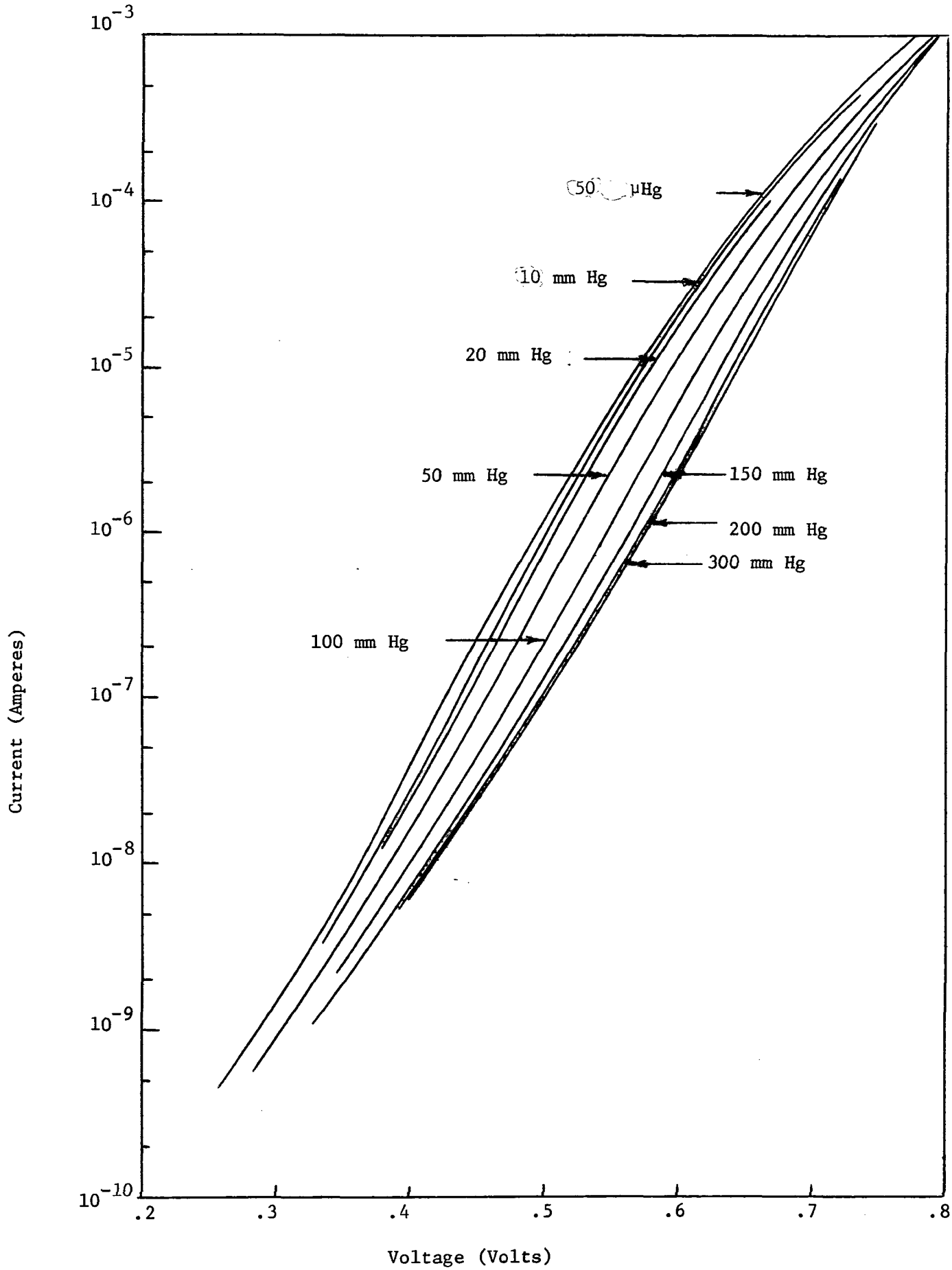


Figure 31. Log I-V Characteristics of Transducer No. 2; Bias Condition 2.

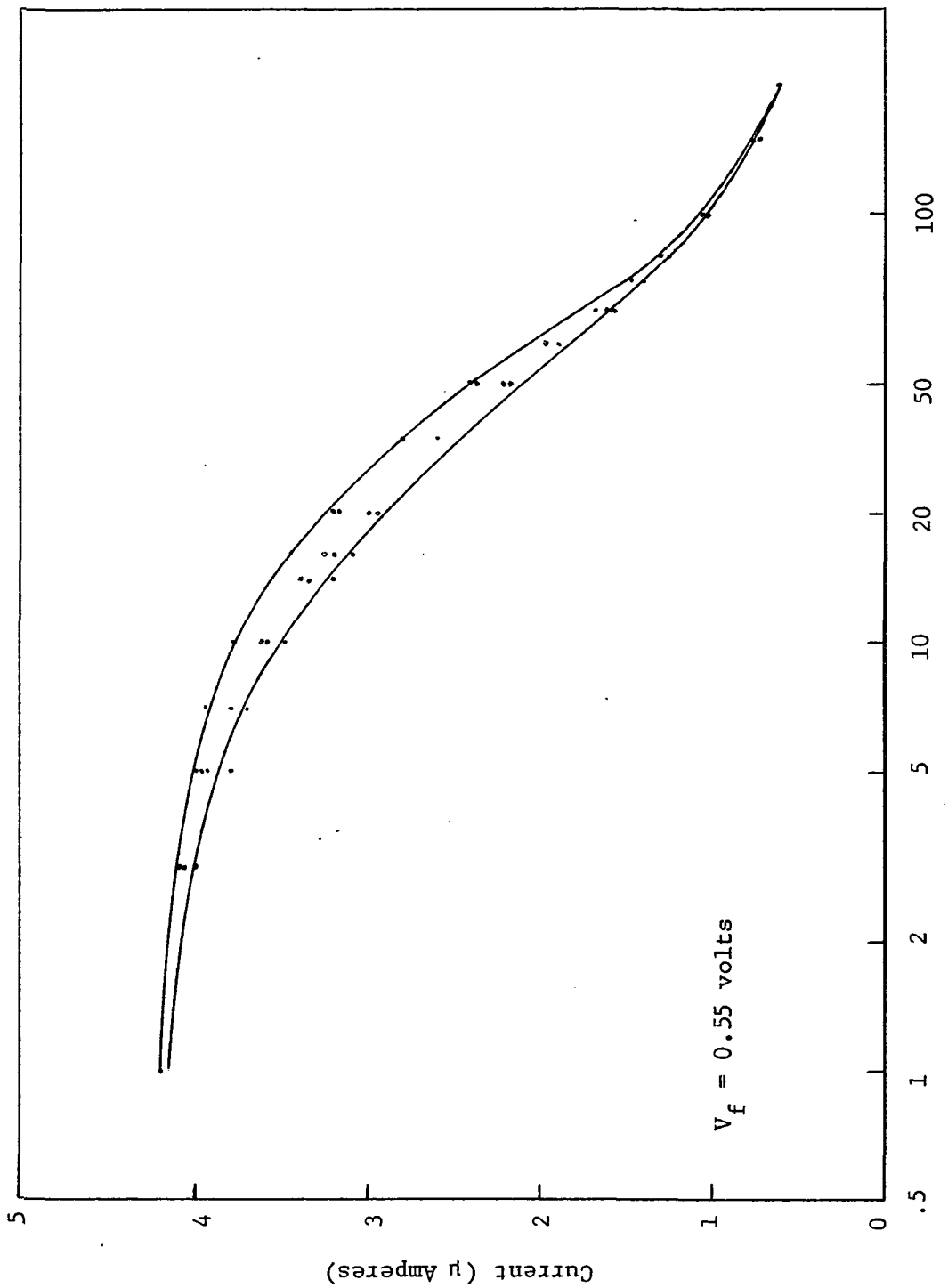


Figure 32. Pressure--Current Characteristics of Transducer No. 2.

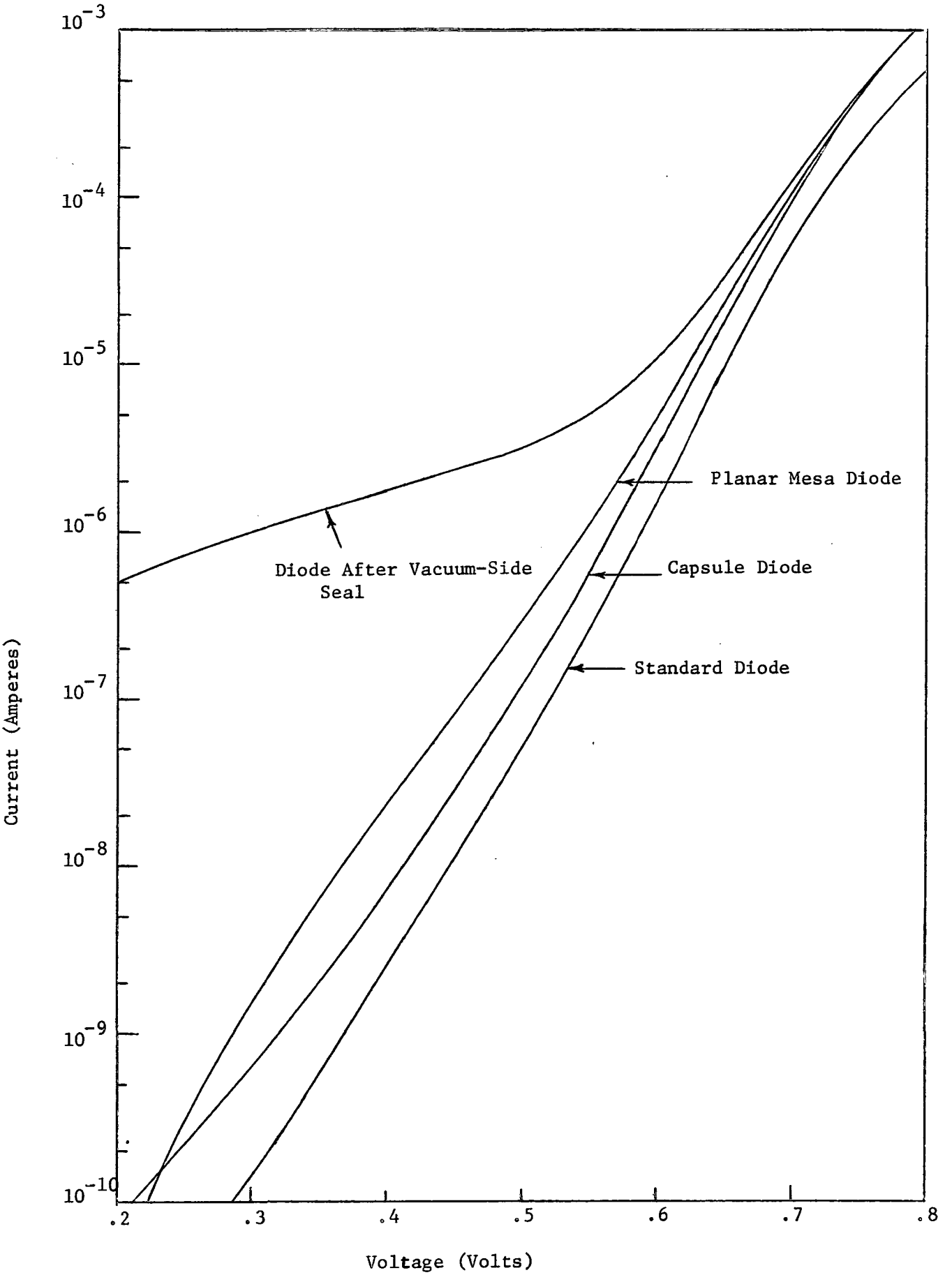


Figure 33. Log I-V Characteristics of Transducer No. 3 Diode at Various Stages.

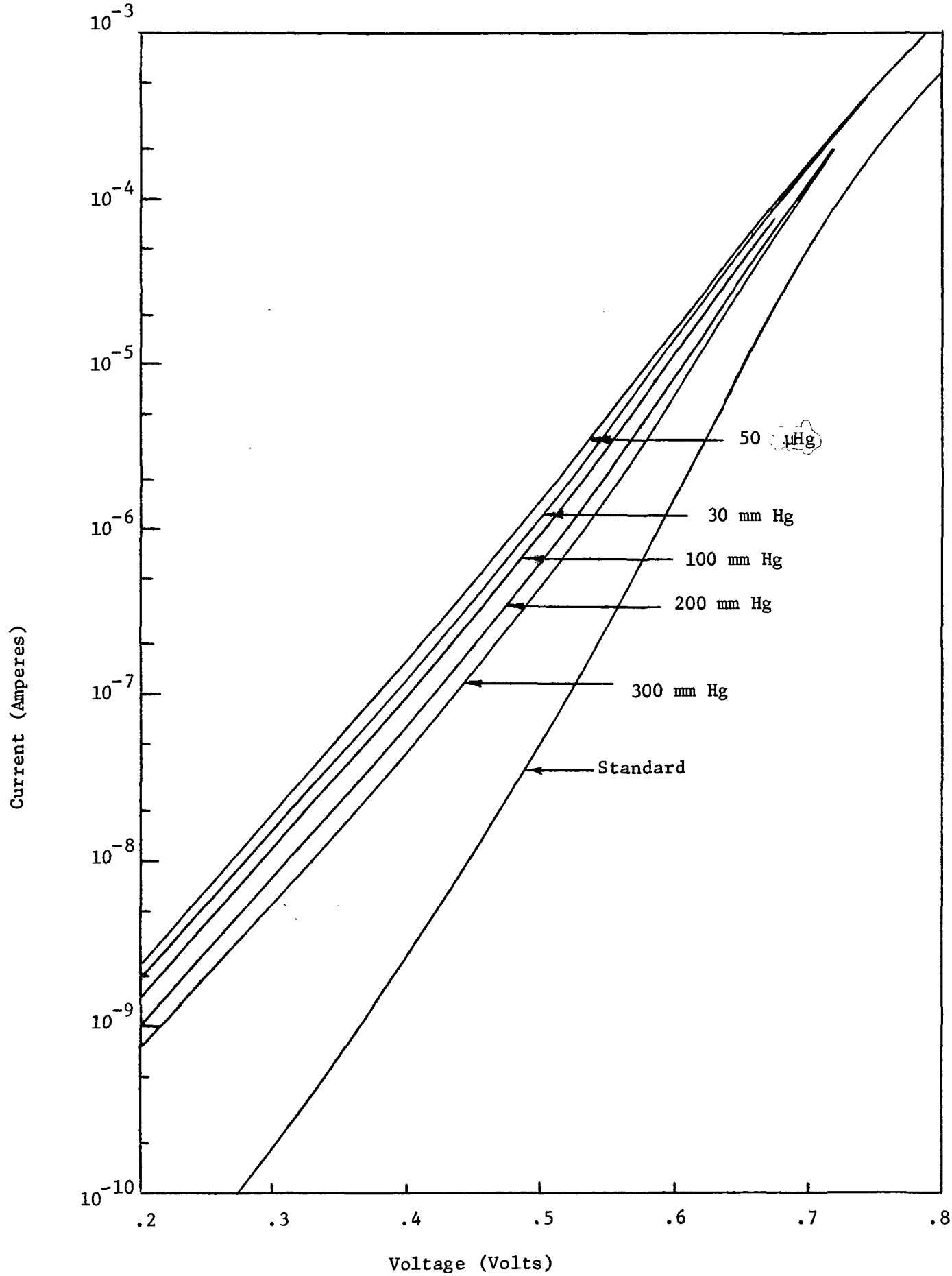


Figure 34. Log I-V Characteristics of Transducer No. 3, Bias Condition 1.

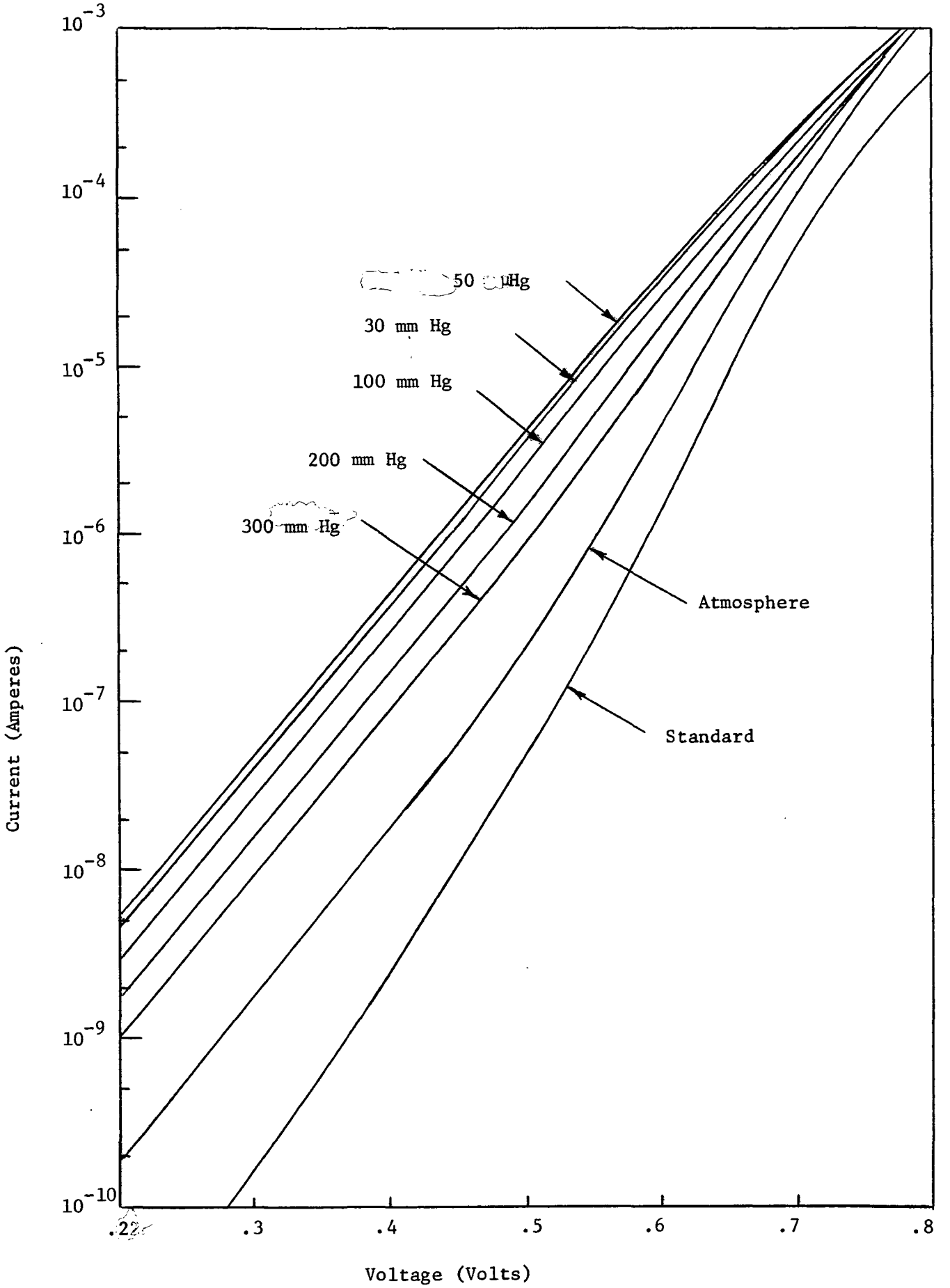


Figure 35. Log I-V Characteristics of Transducer No. 3; Bias Condition 2.

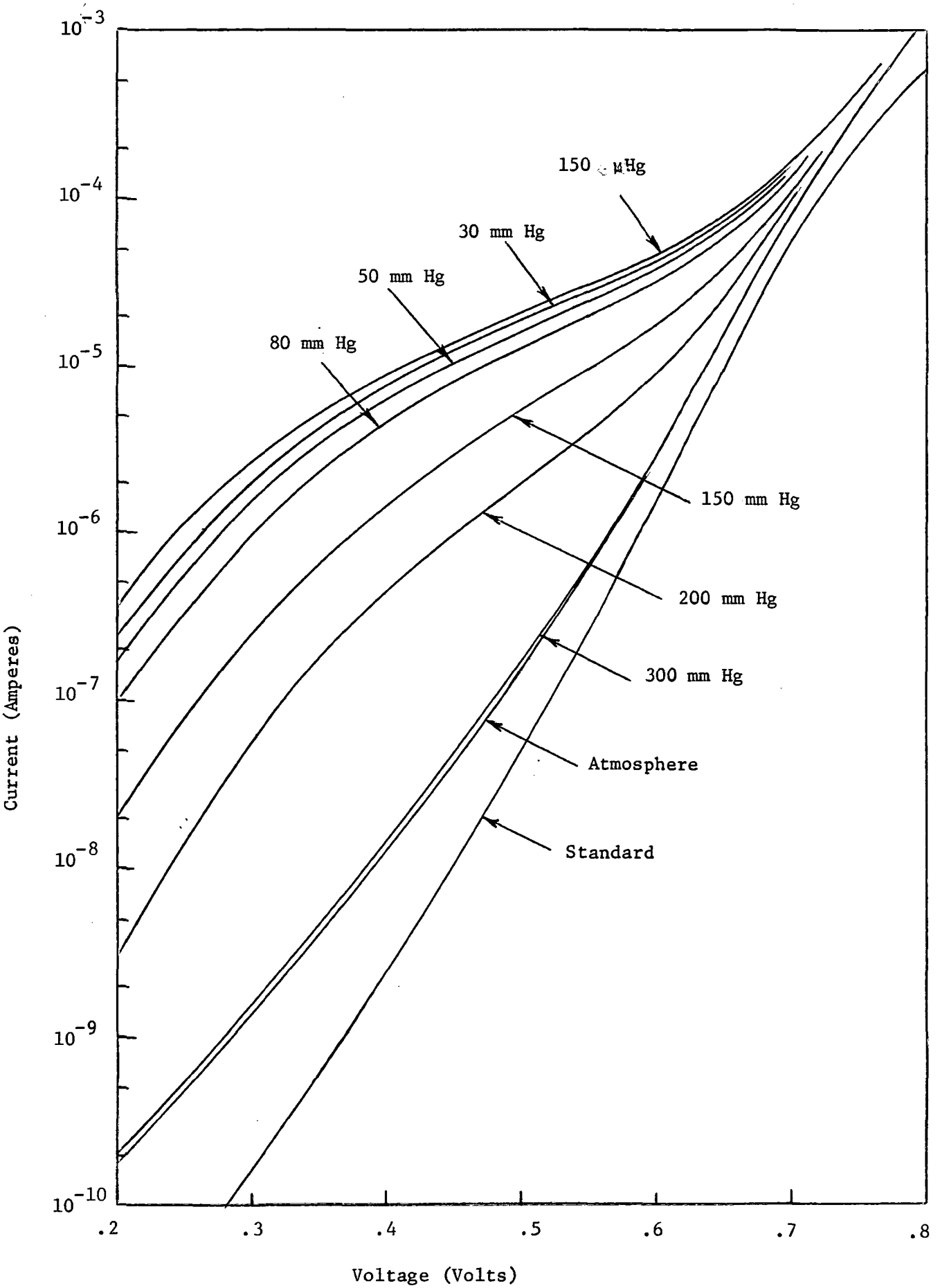


Figure 36. Log I-V Characteristics of Transducer No. 3; Bias Condition 3.

condition, and stress decreases as pressure increases. The limiting effect of the series resistance and other than ideal diode current is evident in each case. Fig. 36 is of interest in that an increased initial bias has yielded an increased sensitivity, but the series resistance restricts the increased sensitivity to low voltage bias levels. At lower voltages, the sensitivity is significantly greater but current changes are more difficult to detect. All of the curves in Fig. 36 appear to approach a constant slope at low voltage biases. If the series resistance effect could be eliminated such that these curves would continue with the initial slope, an extremely sensitive transducer would result.

Transducer No. 3 was broken before additional testing could be completed.

Transducer No. 4

Transducer No. 4 is unique in two respects. 1) The diode used in transducer no. 4 was fabricated in 1-1-1 silicon rather than 1-0-0 silicon. (1-1-1 silicon is known to be less sensitive.) 2) When completed as a capsule diode, the 1-1-1 unit was stress-biased and no additional bias was required. The reason for the bias is unknown, but it probably resulted from thermal expansion during the sealing operation. It was a fortunate incident in that it provided an opportunity to evaluate the capsule diode independently of the housing.

The curves of Fig. 37 show the transducer to be of poor quality. Series resistance is in evidence and the slopes are poor. The curves are of interest basically because two curves are included for each pressure. The lack of repeatability is probably attributable to the floating diaphragm situation described in Section III.

Planar-Mesa Diodes

In order to evaluate the repeatability of the stress V-I characteristics of planar-mesa diodes, the apparatus illustrated in Fig. 38 was arranged. The planar-mesa diodes rested on a flat, hard surface with a glass slide covering the entire structure. In practice, the glass cover was attached to the silicon at one end with a small quantity of adhesive material. A hinged arm, e.g., a phonograph tone arm, was placed on the glass cover directly above the planar-mesa diode and a weight, ω, added until the diode was stress sufficiently to change its I-V characteristics. The diode characteristics were observed as the weight was cyclically added and removed from the tone arm. In each case, the I-V characteristics were observed to be repetitive. Only a few diodes were tested in this apparatus. Neither the tone arm nor the glass cover could be removed and replaced with confidence, and the risk of damaging good diodes was considerable.

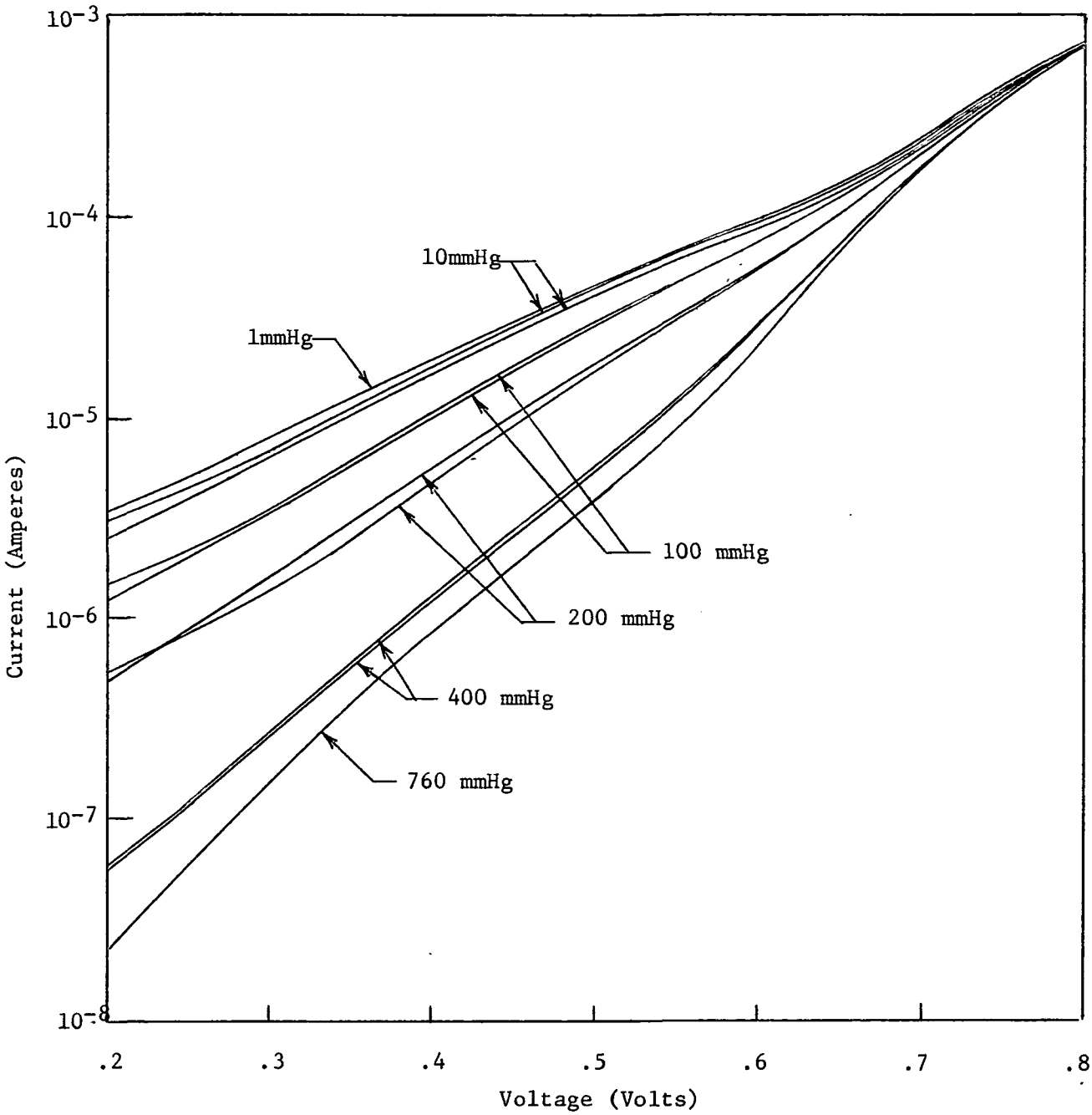


Figure 37. Log I-V Characteristics of Pressure Transducer No. 4

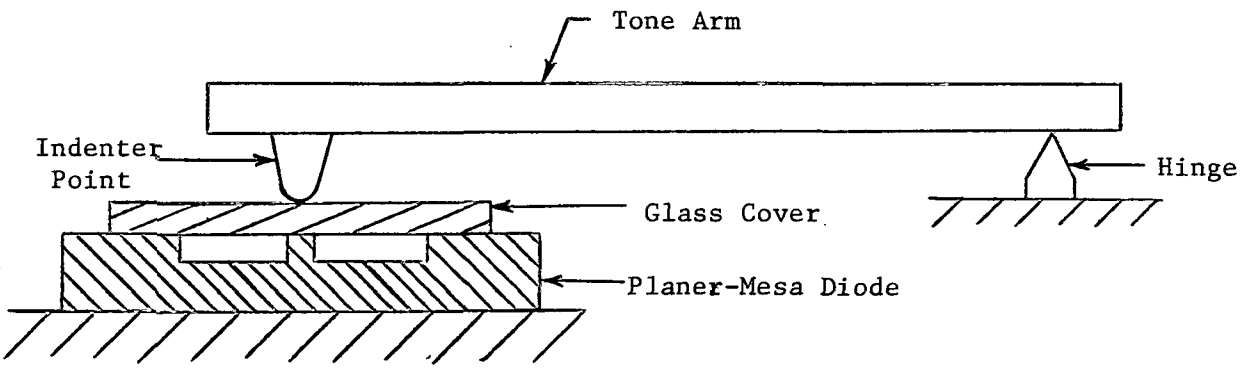


Figure 38. Test Apparatus for Planer-Mesa Diodes.

Instrumentation

Instrumentation for a voltage readout of the piezojunction pressure transducer is illustrated in Fig. 39 where R is equal to the diode impedance at quiescence. Ideally, R' in the bridge circuit would consist of a diode to match the quiescent pressure transducer's impedance, thus providing a temperature compensation element in the bridge. The compensating diode should be located on the same chip in close proximity to the planar-mesa diode. In practice, one of the bridge resistors can be varied to balance the output to zero at quiescence or a conventional bridge balancing network can be used as illustrated.

Consider, for example, the log I-V curves of Fig. 28. As a compromise between maximum sensitivity and the desirability of operating the transducer at a higher current level (less resistance), a forward voltage bias of 0.45 volts was selected for this transducer. At the quiescent point, the transducer has an impedance of $11 \times 10^6 \Omega$. If the bridge circuit resistor, R in Fig. 39, is also $11 \times 10^6 \Omega$, the bridge excitation must be 0.9 volts to bias the transducer diode to 0.45 volts. In Fig. 28, curves are included to show the approximate transducer operating point for series resistor values (R in Fig. 39) of 11×10^6, 10^6 and 10^3 ohms. (These are approximate values because less voltage is available to bias the transducer diode as current is increased due to stress increases). As the transducer is stressed by decreasing pressure, the output of the bridge circuit in Fig. 39 can be estimated by reading the change in the transducer diode voltage on the abscissa of Fig. 28. If R is $11 \times 10^6 \Omega$, for example, the output of the bridge circuit of Fig. 39 will be 0, 0.05 and 0.14 volts at 760, 100 and 30 mm Hg, respectively.

It is generally true that transducers are the less-accurate and less-repeatable element in an instrumentation systems. For a bridge circuit such as illustrated in Fig. 39, amplifiers are readily available to buffer, resolve, and amplify the bridge output signal. The transducers discussed herein were particularly nonrepetitive and a good instrumentation system was of little value. Additionally, these transducers were limited to low forward biases by the series resistance and the quiescent impedance was comparable to the differential input impedance of many instrumentation amplifiers. This was not the case in the needle-diode transducers, for example, and should not be a factor in good-quality capsule-diode transducers.

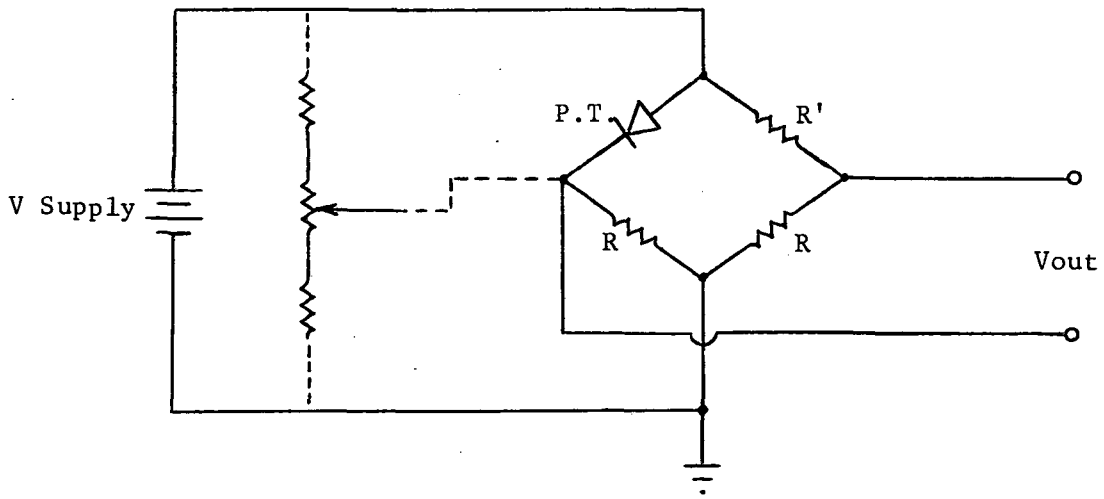


Figure 39. Bridge Readout Circuit for Pressure Transducer.

SECTION VII

CONCLUSIONS AND RECOMMENDATIONS

The piezojunction pressure transducers designed and fabricated during this investigation have several advantages. Unlike transducers fabricated during predecessor contracts, the present design requires only the standard processing procedures of planar silicon technology. Consequently, it is reasonable to expect that the silicon, planar mesa diodes used in the fabrication of these transducers can be mass produced in a production line environment. Other components, i.e., the glass covers, are not unlike existing, readily available glass components. Consequently, it is probable that these are also amenable to mass production. The assembly of these components into the present transducer design is relatively straightforward.

The design also features a built-in vacuum reference and is, therefore, an absolute pressure transducer. The vacuum reference acts so that at one atmosphere of ambient pressure, the stress-sensitive p-n junction is at a minimum of stress. As pressure decreases, stress on the transducer increases and sensitivity increases. The region of maximum sensitivity can be controlled to some extent by the stress-bias adjustment. The transducer also has a large dynamic range. It functions from an atmosphere down to a pressure limited by the transducer's sensitivity, and it cannot be damaged by overpressure in the region below an atmosphere.

The transducers fabricated have not been impressive in performance. They were functional only at low current levels (low forward bias voltages), and their pressure-I-V characteristics were unrepeatable. The primary reason for these disappointing results is that only poor quality diodes were available for transducer fabrication. The diodes fabricated were characterized by surface problems (non-ideal currents) and excessive spreading resistance. The mask-set designed to process these diodes required better control over topography than could be achieved in the laboratory processing the diodes. These masks would have been routinely processed in a state-of-the-art laboratory.

It is concluded that the transducer design is also deficient in that the multiplicity of diaphragms is incompatible with the extremely stress-sensitive piezojunction effect. An improved design would restrict the movement of the stress-bias spring and the port-side glass diaphragm once the initial bias was set. This design deficiency is of little significance, however, when compared with the dominant problems of using poor quality diodes.

The results achieved during this investigation do not demonstrate the sensitivity that is theoretically inherent in the piezojunction effect. What is required for such a demonstration are diodes of improved quality such as can be routinely produced in a state-of-the-art laboratory. It is further required that these diodes be fabricated in low resistivity, 1-0-0 silicon. The low resistivity should present no problems since only the forward characteristics are of interest. It is also recommended that any effort to obtain such diodes include plans for a new mask-set to capitalize on the capabilities of a state-of-the-art laboratory. The stressed area to total area ratio can be increased, for example, and a temperature compensating diode can be included at negligible cost. The design can be further enhanced by obtaining other custom parts, such as the glass diaphragms of the capsule diode. Other factors which may be considered are the use of silicon diaphragms in the place of glass, and the use of glass washers to facilitate sealing of silicon to silicon.

A FOLLOW-ON STUDY FOR MINIATURE SOLID-STATE PRESSURE TRANSDUCERS

PART B: December 1970 - June 1974

SECTION I

INTRODUCTION

This part of the report describes a follow-on effort to that of Part A in which the major shortcomings of the effort described in Part A are remedied by employing a commercial vendor for the fabrication of various silicon parts. In addition, the transducer was redesigned and the dimensions of the package changed, although the operating principles and the area and shape of the active element are substantially the same. The major change in the package design of the Part B activity is that the housing and loading elements are all silicon parts which are sealed to each other by the use of electrostatic silicon-to-silicon seals. These electrostatic seals are formed by sputtering a thin layer (between 5 and 25 μm thick) of commercial borosilicate glass (Corning 7740, "Pyrex") on one of the members to be sealed.

Part B is divided into sections as follows:

1) New Technology. Before the new design could be adapted certain basic technological problems had to be overcome. The first was the demonstration that silicon-to-silicon seals were a practical, reliable method for joining silicon surfaces together.

2) Design. To take full advantage of the new technology and to produce a unit responsive to the needs of the rocketsonde program a new design was developed to enhance sensitivity over previous units. This design insures that the maximum sensor sensitivity occurs in the low pressure regions at which the need for better pressure measurements is the greatest.

3) Fabrication. The procedures used to fabricate the prototype test units deviated somewhat from those initially planned. These deviations and the reasons for them are reviewed in this section along with a summary of the entire fabrication sequence.

4) Results. The performance of those units fabricated using the new design and technology are summarized along with a discussion of the major shortcomings still remaining.

SECTION II

NEW TECHNOLOGY

One of the goals of this new research was to develop a silicon element housed in an all-silicon package. The use of an all-silicon package seems advantageous in the construction of piezojunction elements because of the mechanical properties of the silicon itself. In a piezojunction device incorporating a planar mesa active element, a silicon mesa presses up against a flat surface to produce stress levels on the order of 5-50 x 10^9 dynes/cm^2. At these high stress levels most materials deform, including borosilicate glass elements such as have been used in previous designs. Silicon, on the other hand, has been shown many times now to be able to withstand stress levels of this magnitude with no deformation or yield in mechanical properties, even though such stress levels are above the usually quoted values of the fracture stress of silicon. The explanation apparently lies in the fact that the published values of fracture stress are really defect limited as these values have been determined on relatively large samples with a high probability of including significant defects. On the other hand, piezojunction structures built into very small, relatively defect-free areas can tolerate stresses an order of magnitude or more above the published fracture stress of 3-4 x 10^9 dynes/cm^2. Consequently, silicon itself is an ideal material not only for building the piezojunction device, but also for applying the forces that cause the properties of the piezojunction device to change.

The present design then had as a goal a structure which would include a silicon-to-silicon loading configuration unlike previous designs which included Pyrex loading members. In order to make such a loading arrangement possible two conditions had to be fulfilled:

1) Electrostatic silicon-to-silicon seals must be feasible if the design is to retain the Mallory electrostatic sealing technique as a means of achieving a hermetically-sealed absolute reference enclosure;

2) The technology for forming such seals and shaping the members that constitute the elements of the seal must be compatible with the dimensions required for diaphragm displacement and loading.

Both of these conditions were adequately met as discussed in the following subsections.

Silicon-to-Silicon Seals Using Sputtered Borosilicate Glass

What was well established in the electrostatic sealing art at the beginning of this program was that silicon-to-Pyrex cavities were a reliable, relatively easy to make type of seal which showed good heremeticity and excellent mechanical properties. Such seals have been used to form piezoresistive pressure transducers and as such have exhibited hysteresis comparable with the best commercial units in the field, including those based on high temperature silicon-to-silicon seals. The advantage of electrostatic sealing over other methods for making silicon-to-silicon seals is that the electrostatic technique is the only technique which can be carried out at temperature of 500°C or less. The "conventional" methods for making silicon-to-silicon seals employ a combination of high temperature and high pressure which render them incompatible with assembly of devices already metallized with aluminum, for example.

Making electrostatic silicon-to-silicon seals requires a glass layer as an intermediate sealing region between the two silicon members. The composition and mechanical properties of this layer are highly important for a successful seal. The initial attempt was to prepare a glass similar in properties to those of Pyrex which had been so successful in the previous sealing work.

The first technique investigated for preparing such layers was to heavily dope a thermally grown oxide with boron and thereby produce an oxide glass layer similar in major constituents to Pyrex (~ 78% SiO_2, 20% B_2O_3, 2% other). To do so we prepared thick (on the order of 4 μm) layers of borosilicate glass by oxidizing silicon at 1250°C for 16 hours in a steam atmosphere generated by bubbling nitrogen through a hot, boric acid solution. The oxide layers resulting from such a procedure were hard, clear and quite glassy in appearance but none of these layers were successfully sealed. Rather than incrementally modify the composition of the thermally grown oxide to zero in on a layer with the desired properties, the decision was made to select the deposition method that would reproduce the Pyrex layers as accurately as possible. The technique that seemed to offer the best hope for doing so was that of sputtering which was therefore investigated next.

A five-inch target of Corning 7740 Pyrex was purchased from MRC* and used in conjunction with an MRC 340 sputtering unit made available to us through the courtesy of Dr. M. A. Littlejohn at North Carolina State University. This apparatus has the capability of depositing between 50-100 Å per minute of glass at a pressure of 5×10^{-3} Torr. Initially, we deposited the Pyrex as an overcoat on a 4 μm thick layer of thermally grown SiO_2. This procedure resulted in films which drew substantially no

*Materials Research Corporation, Orangeburg, New York.

current at voltages up to 300 or 400 volts at which point sudden shorting occurred. The explanation assumed was that the applied field appeared primarily across the thermal oxide until a breakdown occurred at a defect or pinhole in the thermal oxide causing all subsequent current to flow through the very small number of defects. This action prevented any sealing from occurring with such thermal oxide-Pyrex sandwich combinations.

The next attempt was to sputter the borosilicate glass upon an essentially oxide free surface of silicon. This surface is prepared by etching the silicon in concentrated hydofluoric acid. A thin oxide does reform prior to the sputtering but this oxide is between 2-3 nm thick and hence is negligible in resistance compared to the much thicker borosilicate glass deposited on top of it.

When the substrates were coated in this manner, polished silicon could be electrostatically sealed to them. The procedure is similar to that previously developed for silicon-to-Pyrex seals, although the voltages are lower and the temperature during sealing is somewhat higher. With the 4-6 μm thick films investigated initially an important step prior to sealing was to anneal the sputtered borosilicate glass film at a temperature of 600-900°C. We found a slightly higher yield when this annealing was carried out in steam, but successful seals were formed after annealing in either nitrogen or oxygen. Failure to anneal these thin films resulted in less satisfactory results in that the areas of sealing tended to be discrete and patchy and incompatible with the formation of hermetic enclosures. Later, thick Pyrex films (10-25 μm thick) sealed satisfactorily without any post deposition annealing.

To evaluate the hermeticity of these seals a structure was fabricated in which a cavity was sealed to a lid, the lid being thin enough to produce a visible depression when the sealing was carried out in a vacuum and then returned to atmospheric pressure. This sealed cavity unit was subjected to helium leak testing and showed substantially zero measurable leak rates by this instrument. Appendix D reproduces a note published in the Journal of the Electrochemical Society describing the electrostatic silicon-to-silicon seal. This method is attractive, not only for sealing piezojunction elements, but also for sealing piezoresistive elements such as those illustrated in the JECS paper. The fact that such seals have been shown to be hermetic and largely creep-free makes them suitable for housing all kinds of pressure sensing semiconductor elements.

Housing Considerations

The housing configuration for the sensor is shown in Fig. 40. This sketch represents a cross-section of the all-silicon package. This

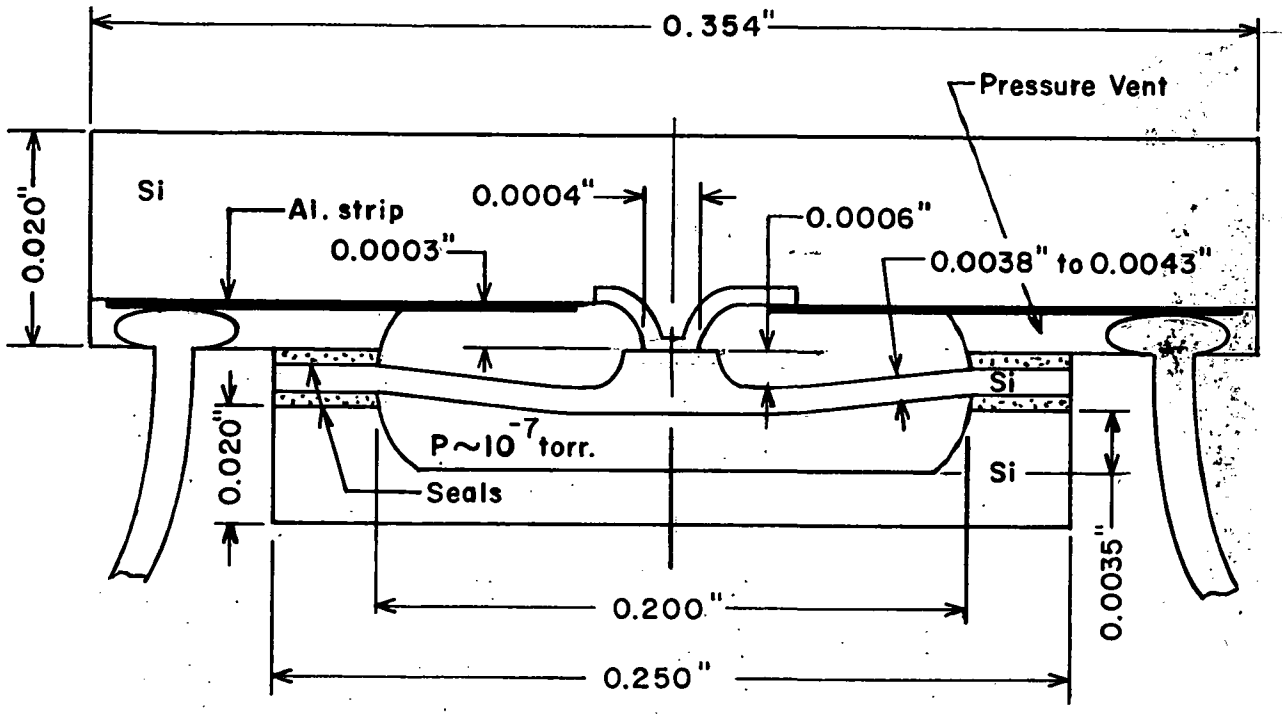


Fig. 40. Illustration of the Housing Configuration.

structure is quite similar to those previously fabricated (see Figs. 12 and 13, Part A), but differs in the following important respects:

1) all elements of the structure are silicon and are joined together by silicon-to-silicon electrostatic seals;

2) the active diode element is located in the thick, non-flexible top member of the three-member package.

The dimensional control required to fabricate this structure is extremely demanding. To be successful the deflection of the thin diaphragm member must be great enough to allow for the added thickness represented at the rim by the sealing glass. Too little deflection means that the diode most likely will be damaged during sealing; too much deflection means that the diaphragm mesa will not contact the diode until the very lowest portion of the intended pressure range. Consequently, the process used to form the mesa on the diaphragm member and to deposit the sealing glass must be under good dimensional control.

The assembly sequence of the various members is as follows:

1) The thin diaphragm member is sealed first of all to the substrate cavity member. This sealing is carried out at high vacuum so that when the sealed assembly is removed from the vacuum, the thin member deflects under atmospheric loading.

2) The second step is to seal the top silicon member, containing the active diode element, to the already sealed diaphragm cavity assembly. This sealing operation is carried out at atmospheric pressure or conceivably above atmospheric pressure. The key dimension of concern here is that the top of the mesa in the diaphragm member be no higher than the top surface of the sealing glass on the periphery of the diaphragm. Meeting this condition means that the piezodiode should not be in contact (loaded) during the top sealing operation.

3) Following sealing, however, the spacing between the mesa on the diaphragm member and the top of the active diode mesa should be sufficiently small that under reduced pressure the unloading of the diaphragm causes the diaphragm mesa to exert a force on the planar mesa. This loading action is what produces the piezojunction effect in the diode output.

The processes that are important in determining dimensional control include not only the initial shaping, lapping and polishing operation for the individual silicon members, but also the procedures used to form the mesa on the thin silicon diaphragm member and the procedures used to deposit and control the thickness of the sealing glass. The etching of the bottom cavity member and the etching of the mesa in the top cavity member are unimportant in determining package alignment. The package is designed so as to rely heavily upon the initial flatness of the wafers used to form the package. The top of the planar mesa and the periphery of the active element chip (contacting the sealing glass) lie in the same plane. Similarly for the cavity member, the design assumes only that the initial silicon wafer is flat to a tolerance small compared with the deflections involved.

Methods for controlling the thickness of the sputtered layer are generally adequate, although procedures are not available for measuring film thickness in situ--unlike the monitoring methods commonly used with evaporated layers. Mass monitors continually measure the buildup of mass on a surface within a vacuum chamber while the evaporation process is going on. Such mass monitors do not operate successfully in a sputtering atmosphere because of the difficulty of positioning the monitor in a meaningful location and also because of the high voltages and charged particles involved in the sputtering operation itself. Temperature also is an important factor in measuring film thickness by the mass monitor.

The technique used here involved none of these monitors but simply resorted to empirical curves based upon the time and power levels during sputtering.

SECTION III

DESIGN

The performance desired of the sensor is the measurement of absolute ambient pressure over the range between approximately 700 Torr and 10^{-2} or 10^{-3} Torr. This goal sets an extremely wide dynamic range and the emphasis within this range is on the lower pressures. Consequently the loading strategy adapted is similar to that previously used (see Section III of Part A). This configuration has the advantage of putting the maximum stress on the diode at the lowest ambient pressure to be measured; that is, the diode exhibits its greatest sensitivity in the region of lowest pressure and hence is better able to respond to small changes in low pressures than if the mesa load became smaller as the atmospheric load decreased.

The dimensions settled upon for the present design are shown in Fig. 40. The area of the diaphragm to be loaded is approximately 2×10^{-5} meters^2. At atmospheric pressure of 10^5 N/m^2, the total force appearing on the diaphragm is approximately 2N. Since only 1/5 of this force is supported in the center, the expectation is that with these nominal dimensions a total force of 0.4 N should appear on the center mesa. If the mesa itself is 1/2 mil in diameter, the total stress appearing normal to the top of the mesa should be approximately 3.2×10^9 N/m^2 (3.2×10^{10} dynes/cm^2) which, according to Fig. 9 of Part A, should produce a change in the current flowing through the diode of about 200. Figure 9 assumes a ratio of stressed diode area to total area of 0.175. This ratio is typical of the diodes being fabricated in Part B. Because of the "dead space" built into the transducer, a full atmosphere will never appear on the planar mesa but rather some fraction thereof.

The deflection of the diaphragm can be calculated from Eq. 29. Assuming m is equal to 3, the deflection at the center of the diaphragm under one atmosphere of pressure should be between 5 and 7 μm depending upon the exact diaphragm thickness. The glass layer thickness was specified as 8 to 10 μm in this design. The height of the diaphragm mesa was typically 15 μm ± 2 μm. Consequently most of the diaphragms should align with the top member so as not to contact the planar mesa diode until the ambient pressure falls substantially below 1 atmosphere.

The geometry of the various members is illustrated in Appendix E which is a description of the mask set ordered from a commercial vendor, as well as a general processing description.

SECTION IV

FABRICATION

The design described in section III requires three silicon members to complete the package, one of which also contains a planar mesa diode whose changing properties with load act as the sensor for the pressure transducer. The three members of the transducer are: 1) the cavity member, 2) the diaphragm member, and 3) the active element member. All silicon and photomasks for the fabrication of the pressure transducer were furnished by Siliconix, Inc., Sunnyvale, California. For the cavity member and the diaphragm member, 30 silicon wafers of each thickness were supplied along with the photomasks necessary to etch cavities or mesas in the silicon. For the active element member, Siliconix furnished the silicon and the photomask and also carried out all processing up to and including metallization. This means that Siliconix etched the planar mesa diodes for the active element using a mask which not only forms the mesa but also provides vents whereby the transducer equilibrates with the ambient pressure. The mask also provided large areas of bare silicon for electrostatic sealing by which the active element is attached to the other members of the transducer.

Fifty active element wafers, containing 25 active element chips each, were provided by Siliconix.

RTI's task in the fabrication consisted of: 1) etching the cavity members so as to form a reference pressure cavity; 2) etching the diaphragm members in order to form a diaphragm mesa which loads the planar mesa; 3) coating both the cavity members and the diaphragm wafers with borosilicate glass in order to carry out the electrostatic sealing; 4) dicing the wafers into individual chips; 5) carrying out the transducer assembly with appropriate electrostatic seals either in vacuum or in atmospheric nitrogen; and, 6) mounting, wire bonding and testing the completed transducers.

Cavity and Mesa Etching

The technique used to etch the silicon into the desired geometry for both the cavity member and the diaphragm members followed that described previously in earlier piezojunction work (Refs. 11,12). The etch of the cavity member is not precise in that the amount of silicon removed is relatively unimportant. What is required is a cavity deep enough to not interfere with the diaphragm motion during the transducer assembly and operation. The volume of the cavity should be as large as possible so as to reduce susceptibility to

outgasing or microleaks. In practice the depth of the cavity was approximately 3 mils. This depth was limited by the thickness of the thermal oxide grown on the silicon wafer which forms a mask during the silicon etch. The procedure used consisted of growing a 2 μm thick layer of SiO_2 on the starting silicon wafer. A pattern was cut in this oxide using standard photoengraving and oxide etch methods. The photoresist was then removed and the resulting oxide mask used to define the geometry during a subsequent silicon etch. The silicon etch consisted of 180 ml HNO_3, 30 ml acetic acid and 24 ml HF. This etch attacks silicon much more rapidly than it does the oxide, but it does attack the oxide and attempting to go deeper than 3 mils appeared to run the risk of etching the top surface as well. Since satisfactory electrostatic sealing depends upon near optical flatness, it would be highly undesirable to etch this surface. Consequently, the etch was stopped before all oxide was removed.

Because of the high doping level of the P-type substrates (these wafers are 0.02 ohm-cm type) the HF/HNO_3 acid used to etch the silicon frequently leaves a dark stain on the silicon surface, much like the stains characteristic of junction delineation in HF rich solutions. This stain was removed by heating the wafers in the oxidation furnace (100 percent oxygen atmosphere) for 15 minutes at 1000°C degrees. This procedure oxidized the silicon uniformly and upon subsequent oxide etch, removed the freshly grown oxide which had uniformly consumed the silicon-rich, dark stain. Following this step, the silicon surface appeared clean and highly reflective.

The etching of the diaphragm member was carried out similarly, except that the oxide thickness was 7000 Å since the depth of the etch was much less. Typical mesa heights were 12 to 15 μm. Again the need to remove the dark stain existed and the same procedure used for the cavity members was carried out here. Actually on the cavity members, stain removal is unimportant since the stain is confined to the bottom of the cavity. On the diaphragm members, however, it is the etched surface onto which the glass layer will be sputtered. No evidence exists to show that this stain either adversely affects the adherence of the sputtered layer or compromises the hermeticity of the seal between the sputtered layer and the silicon. These possibilities were not investigated because an easy method for removing the stain was available.

Controlling the height of the mesa is critical in the fabrication of the diaphragm units. Consequently, the etch rate was determined on blank wafers immediately prior to etching the production wafers. By this method, uncontrolled variations in the etch rate were empirically accounted for and relatively good control of the desired mesa heights was thereby achieved.

Coating

The next step in the assembly sequence is to coat the cavity member wafers and the diaphragm member wafers with a glass layer suitable for making the electrostatic seals previously demonstrated (see Section II, New Technology and Appendix D). Electrostatic sealing at the beginning of this contract was carried out using sputtered borosilicate glass layers. This process is a lengthy one involving anywhere between 20 to 40 hours of sputtering time and the number of 2 inch diameter wafers that can fit beneath the 5 inch diameter target is very limited, particularly when the thickness of the sputtered glass layer is critical. One of the intermediate tasks of the program was to develop methods for speeding up the sputtering process. This investigation took place after the feasibility of silicon-to-silicon seals via sputtered borosilicate glass was demonstrated and after a transducer design based upon this technique was completed. Increasing the rf power, varying the temperature of deposition and varying the composition of the residual gas constituting the plasma did not provide a satisfactory solution with the desired enhanced deposition rate. Putting down films at much faster rates generally degraded the necessary smooth surface texture and oft times produced films of poor dielectric properties. In all cases it produced films of less than desirable sealing properties. Portions of this development were performed by the Materials Research Corporation, who used the RTI target (purchased originally from MRC) to deposit films at much higher rates. For various reasons, none of the rapidly-deposited films proved satisfactory for the transducer fabrication. The only successful transducer fabrication has been with films sputtered over a long period of time at relatively low rf power. (~ 200 watts). Typical deposition rates were 0.20 to 0.25 μm per hour. Pressure during deposition was always 5×10^{-3} Torr for the sputtering carried out at North Carolina State University.

As an alternative method for depositing the sealing glass, a brief investigation of chemically vapor deposited borosilicate glass was attempted. This attempt was also carried out by Materials Research Corporation using a high volume production piece of equipment specially designed for depositing glass layers in microelectronics [Ref. 13). This apparatus is capable of coating twenty-five 2 inch wafers in one deposition run and because of the planetary motion of the substrates during deposition, results in a well controlled, highly uniform film thickness. Unfortunately, wafers so coated, while satisfactory in every other respect, failed to produce electrostatic seals. The primary problem is that the current flow during the sealing is extremely low. This same property characterizes thermally grown silicon oxide on silicon. Such dielectric properties are ideal for silicon devices but complicate the electrostatic sealing of oxides/glasses. The corrective action may be to incorporate some alkali or current carrying ions into the deposited glass. The mixture deposited by MRC consisted only of 18% B_2O_3 and 82% SiO_2. With the addition of some sodium or calcium oxide, the conductivity of the glass should increase and the ion motion during the electrostatic sealing most likely would again produce the extremely high electrostatic forces which seem necessary in order to form the high quality hermetic seals. No attempt to modify the chemical vapor deposition technique along these lines was made.

The long tedious sputtering process was reluctantly adopted for coating all wafers for this project. Initial production sputterings were carried out in the apparatus located in the IRD division of Langley Research Center under the general direction of Chris Gross and Rudy Olive. This apparatus incorporates adequate guards and monitors to permit overnight operation unattended.

The RTI borosilicate glass target (a 5" disk of Corning 7740) was used with the IRD system. On occasion, the rf power shut off during the course of an overnight run. This interruption caused problems both in the electrical properties of the film and film thickness control until a timer was installed. The timer recorded the moment of power interruption, and by not breaking vacuum, the rf power could be restored at a later time to continue the run. On one run, the wafers were unloaded after such a power interruption and measured for film thickness. When these same wafers were subsequently reloaded and the run continued, the electrical properties of the deposited glass were sufficiently changed to impede electrostatic sealing. With the technique of not breaking vacuum in the event of power interruption, the film properties were much more satisfactory.

Later sputterings also carried out at Langley Reserach Center, employed a 6" target in a sputtering system of the FID division. These sputterings were carried out by Charles Hardesty, the project contract monitor. Most of the targets used on this system were assembled at Langley by epoxying a 6" disc of commercially-available 7740 glass to the target holder. Targets were changed frequently as the electrical resistivity of the sputtered films tended to increase as the number of runs increased. The final target used was one prepared at MRC using a metallic bonding technique. Inadequate data exist to comment on the aging properties of this target.

Thickness control was by time and power setting only. No in situ measurement of glass thickness was available during sputtering. Thickness control on the cavity members is unimportant so long as the film is uniform. In general the cavity members were coated with 15 to 25 μm of borosilicate glass. The time of the sputtering was nominally 80 hours carried out over a weekend.

The diaphragm wafers require close control on the thickness of the borosilicate glass film. The design of the transducer demands that the following relationship holds: diaphragm mesa height $\leq$ diaphragm wafer glass thickness plus diaphragm wafer deflection during the sealing of the active element chip (generally carried out at one atmosphere). If the mesa height is greater than the sum of the glass thickness plus the diaphragm deflection, the planar mesa diode on the active element will be loaded during the sealing operation and because of the forces involved will most likely be destroyed. On the other hand, if the diaphragm mesa height is less than the diaphragm glass thickness, the two mesas will never come into contact and the output of the transducer will be insensitive to pressure. Between the two extremes is a 6 to 7 μm deflection which allows some tolerance for variation in dimensional control. The magnitude of the transducer dead band depends

upon the dimensions of a given transducer. For the present development, no consideration was given to this problem, the emphasis being on producing prototype transducers that operate over a portion of the pressure range of interest.

Controlling the variables of sputtering (time, power, and temperature) proved adequate to control the thickness of the final sputtered layer to an accuracy of $\pm$ 2 μm.

Only one diaphragm wafer was coated at a time in order to improve uniformity. The cavity wafers were diced prior to sputtering and 100 or more cavity members were sputtered at one time.

Dicing and Glass Etching

The next step in the fabrication sequence was to dice the wafers into individual chips. For the cavity wafers, the dicing into chips generally preceded the sputtering. By dicing prior to sputtering, the edges of all chips are coated with the same glass used to coat the top surface. In addition, having each wafer previously diced into 25 chips enables the sputtering run to coat four to five wafers simultaneously. Without dicing prior to sputtering, this load would be far too great. For the diaphragm wafer, only one wafer per sputtering run was attempted in order to maintain high uniformity of thickness.

The dicing of each wafer into its constituent chips was carried out on a wire saw. Because of the previous wafer etching, all wafers contained small grooves in the surface which formed a starting notch or track for the wire blade during the sawing operation. The sawing operation was chosen as the preferred dicing tool because of the relatively clean edge formed by the saw (as opposed to a diamond scribe for example) and for the relatively good dimensional control thereby made possible. Wear on the wire blade during sawing was severe and wires that started out as 10 mils nominal diameter gradually reduced their thickness to the 5 to 7 mil range before breaking or becoming ineffective. The varying wire thickness plus lateral wire motion during sawing led to 3-4 mil variation in kerf.

Because the cavity wafers were generally sawed and diced prior to sputtering, no further preparation of these chips takes place prior to the first seal. For the diaphragm wafers, however, some processing is necessary. The diaphragm wafers were not sawed prior to sputtering because of the wafer processing that must take place after sputtering.

The first post sputtering operation is the glass etch. The purpose of this etch is to remove the glass from those areas of the diaphragm in which it is not desired. These include the area around the diaphragm mesa.

This mesa is the one that loads the planar mesa diode of the active element yet to be attached. The corner of each chip is also stripped of its glass so that electrical contact can be made in this region during the electrostatic sealing operations.

Mask 6 is the mask designed to facilitate this etching by photoresist methods. Unfortunately, an adequate combination of resist and etch was not developed during the course of this program although several attempts to do so were made. The most serious attempt was a procedure recommended by Kodak for etching Pyrex and claimed by Kodak to be capable of masking up to 1/4 inch of Pyrex etching. This technique consists of coating the glass surface to be etched with an epoxy film and using standard photoresist as a mask on top of that. With an appropriate epoxy solvent, one can remove the epoxy from those area of the glass that are to be etched. The photoresist is then removed and then, with the epoxy acting as a mask for the glass, the unmasked glass is etched. The Kodak combination did not work for us, a major problem being inadequate curing of the epoxy which interacted with the photoresist. Once the interaction occurs, the photoresist loses either its light sensitivity or its solubility in the photoresist developer and the photo lithographic process becomes unworkable. Kodak acknowledged the problem but indicated that, while the curing of the epoxy was critical, it was a process that they felt they had under control. We chose not to pursue this approach further but simply resorted to hand painting a black apiezon mask onto each individual wafer to serve as the glass etchant mask.

After etching the glass layer, the diaphragm was sawed into its constituent chips which are then ready for the initial cavity to diaphragm electrostatic seal.

First Electrostatic Seal

The first electrostatic silicon to silicon seal is between the diaphragm member and the cavity member of the transducer. Both these members are coated with a borosilicate glass layer, the cavity member supporting a thickness in excess of 15 μm and the diaphragm member having an 8 to 10 μm thick layer upon it (depending on the mesa heights). This seal is carried out in a vacuum system. We used an Ultek ion pump to achieve a vacuum on the order of 10^{-7} Torr. A fixture for alignment, made from machineable ceramic (Aremco 720), holds the chips to be sealed in position throughout the sealing operation. The alignment fixture is inside the vacuum chamber and rests upon a heater element which raises the temperature of the assembly to the sealing temperature of ~ 450°C.

The cavity member is loaded into the fixture first with its glass coated side up. The diaphragm member is placed directly on top of the cavity member with its glassed surface also up so that the polished but uncoated surface of the diaphragm chip contacts the glass layer on the cavity chip. This combination is weighted with a blank silicon chip (actually an inverted, dummy cavity member) to which an electrode and weight are afixed. The weight used for this particular seal is 80 grams which is in place throughout the pump down and seal.

At low pressure, the combination is heated to a temperature of 450°C, a dc electric field is applied across the silicon members to be sealed, the diaphragm member being biased positively with respect to the cavity member. The dc voltage is slowly turned up while the current is monitored. Voltage is increased until a current of approximately 10 μA flows. Because of ion motion in the glass, the current drops off rapidly at fixed voltage. Once the current decrease slows down, the voltage is advanced again to build the current back up to 10 μA. This process is continued until a sealing voltage of approximately 250 volts is reached. The assembly remains under bias and temperature for five minutes, after which the heating current is turned off and the sealed members are allowed to cool to room temperature. Upon reaching 100°C, bias voltage is also turned off.

During the sealing operation, the key variable is the current flow through the combination being sealed. This current should show typical ionic current behavior by decreasing rapidly as each new voltage is applied.

Following sealing, the key test for hermeticity is the appearance of a visible depression or dimple in the diaphragm member. This dimple is evident to the eye and results from the atmospheric loading on the thin diaphragm member. Absence of such a dimple indicates that the seal to the cavity has not been hermetic and that no pressure differential exists. Such units are discarded.

Second Electrostatic Seal

The second electrostatic seal is similar to the first with the exception that each cavity-diaphragm combination must be shorted together by an aluminum evaporation on the side. The purpose of this aluminum strip is to electrically connect the diaphragm to the cavity silicon across the borosilicate glass layer.

To carry out the second seal requires that the already sealed diaphragm-cavity combination with the shorting aluminum in place be loaded into the sealing fixture first with the glass side of the diaphragm up. The active element chip which has been processed by Siliconix, but

diced and electrically evaluated by RTI, goes on top of this combination with the diode side down. This chip is oriented so that its corners are rotated 45° from the corners of the combination cavity. (see Fig. 41)

The atmosphere for carrying out this sealing is 100 percent nitrogen at a pressure slightly greater than atmospheric. To create this atmosphere requires simply the flushing of a bell jar with purified nitrogen and carrying out the seal with the nitrogen flowing through. The sealing operation is the same as before.

Tests

After the second sealing operation, the unit is ready for electrical tests. Standard probe measurements and curve tracer displays distinguish between units which have survived the sealing cycles and those which have not.

Those units surviving are placed in 22 lead flat packs using aluminum paint. These units cure overnight and are then wire bonded. With wires in place, the flat pack is mounted on a printed circuit board and subjected to a pressure cycling test in order to establish a calibration curve for the unit.

The calibration system uses a Datametrics pressure transducer for reading the chamber pressures while the electrical output of the unit itself forms the transducer response.

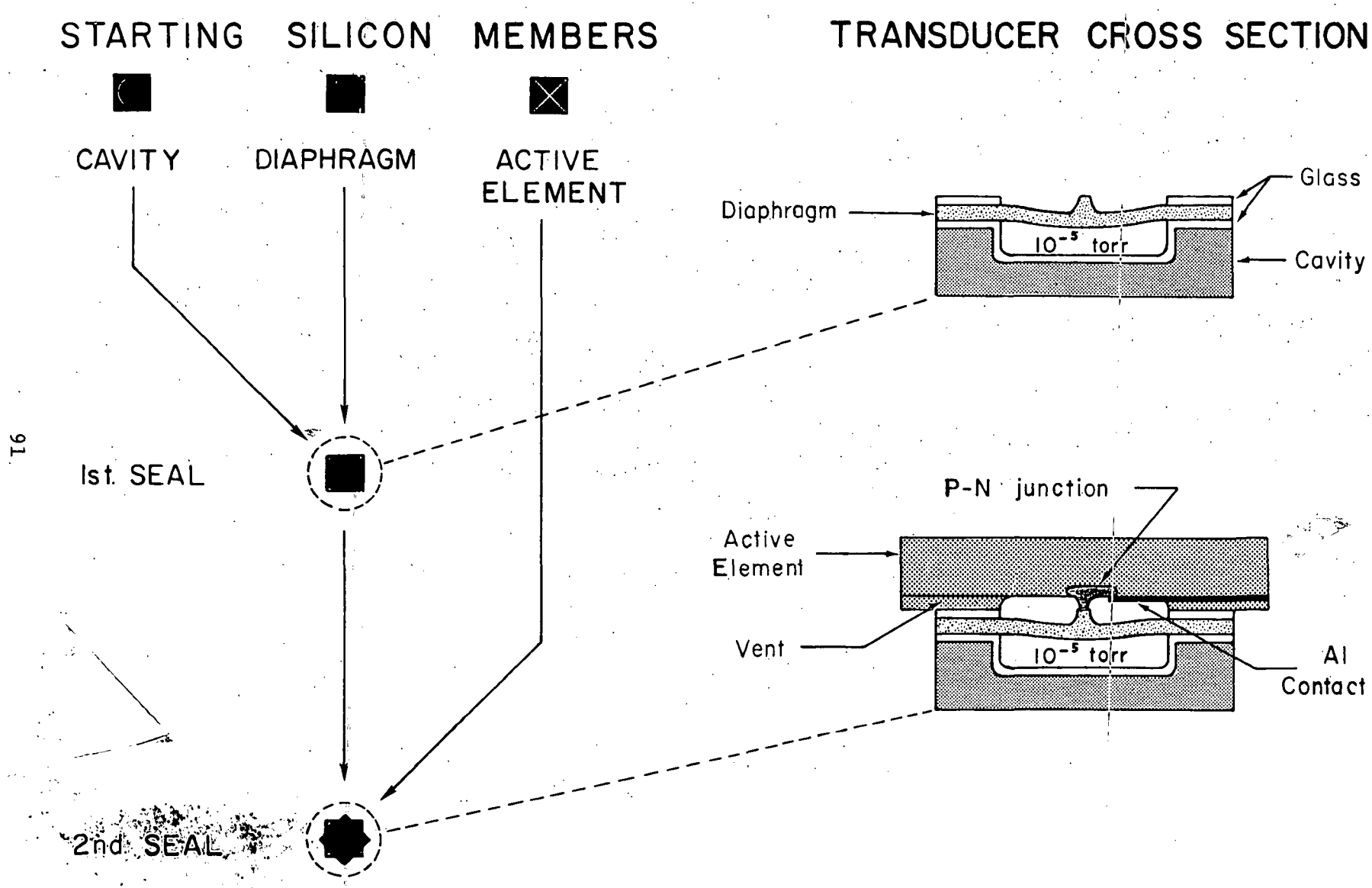


Figure 41. Piezojunction Transducer.

SECTION V

RESULTS

The processing described in Section IV proved to be a low yield process primarily because of losses during electrostatic sealing. Inadequate knowledge of what constitutes a satisfactory sputtered layer with respect to silicon-to-silicon electrostatic seals is a major handicap. The only reliable assessment at present of the suitability of the sputtered glass layer is sealing performance itself. Initial experience suggested this gap would be of minor importance; subsequent experience proved otherwise.

The procedures described in Section IV and Appendix D have been demonstrated to be feasible in separate steps. The complete transducer requires a sequence of steps each of which must be successful in order to produce a useful device.

Initially, yields on the first silicon-to-silicon electrostatic seal (between the diaphragm member and the cavity member) were as high as 25%. Gradually this percentage dropped until suddenly it was zero and a switch in sputtering apparatus was made (Sec. IV). This change partially restored yields on certain runs but not others.

While the second electrostatic seal is not hermetic, it must be mechanically sound. The sealing must occur at temperature low enough to preserve the properties of the planar mesa diode.

Using this initially developed process, we were unable to produce any transducersthat exhibited useful electrical properties. The major losses occurred at the first silicon-to-silicon seal which must be hermetic. The second electrostatic seal, demanding as it does a suitable glass layer on the diaphragm, eliminated most of those units surviving the first seal. Those few units that did possess satisfactory seals at both interfaces showed severely degraded junction properties.

To improve this dismal record two changes were made:

1) The silicon cavity was replaced by a Pyrex cavity, ultrasonically machined from Corning 7740 stock; and

2) The multi-position Ultek sealing fixture was abandoned in favor of the single position carbon strip heater.

The first modification eliminated the need for a sputtered glass layer in order to make the critical first seal. Bulk Pyrex seals easily and reliably with the electrostatic technique. This modification therefore converted the very low yield diaphragm-to-cavity seal into a relatively high yield operation.

The second modification replaced the newly designed and inadequately checked fixture of the Ultek with a thoroughly tested and familiar sealing fixture. With the latter, allowed temperature settings are much better known so that the chances of over heating the active element are greatly reduced.

These two changes established a procedure capable of producing transducers with much improved yield but at a slower rate (this modified procedure is a one-at-a-time method).

Three transducers so fabricated have been tested. These three are the first three successfully produced by the modified process which over a very brief span operated at better than 25% yield--more than one-fourth of the transducers starting the fabrication cycle finished it as working transducers. Prospects therefore are much better with this procedure than the initial procedure. However, the major fault in the initial process stems primarily from inability to deposit a glass layer compatible with high yield hermetic electrostatic sealing. This shortcoming should be overcome with improved process understanding. Highly desirable from a production standpoint would be the development of a rapid method of deposition which required neither the time nor the low pressures associated with the sputtering process. Such a development would most likely have to precede any further commitment to production of these transducers by either process.

Transducer 29-1

The static current-voltage characteristics of transducer 29-1 are shown in Fig. 42. This display is similar to that used in Part A. The equipment and technique for recording these plots are the same.

The curve labelled "COMP" is that of the planar compensating diodes surrounding the planar mesa. All other curves are characteristics of the planar mesa recorded at the indicated value of the ambient absolute pressure. As with the other transducers tested, data were not recorded at the lowest values of pressure (10 torr to 10^{-3} torr) because of limitations in time and also unwillingness to stress these initial transducers to their fullest before complete testing at restricted pressure. However, the testing range covered in Fig. 42 represented about 97% of the maximum load that 29-1 will operate over so that transducer failure because of stress overload is very unlikely for this particular transducer.

The I-V characteristics in Fig. 42 show that the planar mesa diode is not as high a quality diode as the planar compensating diode right next to it. This conclusion is based on the lower slopes exhibited at low voltage by the planar mesa characteristics. The recombination current evident in these non-ideal slopes probably originates at the surface much the same as was found in the analysis of Part A. Note however, that these properties are still generally superior to the characteristics shown in Figs. 25-37. While

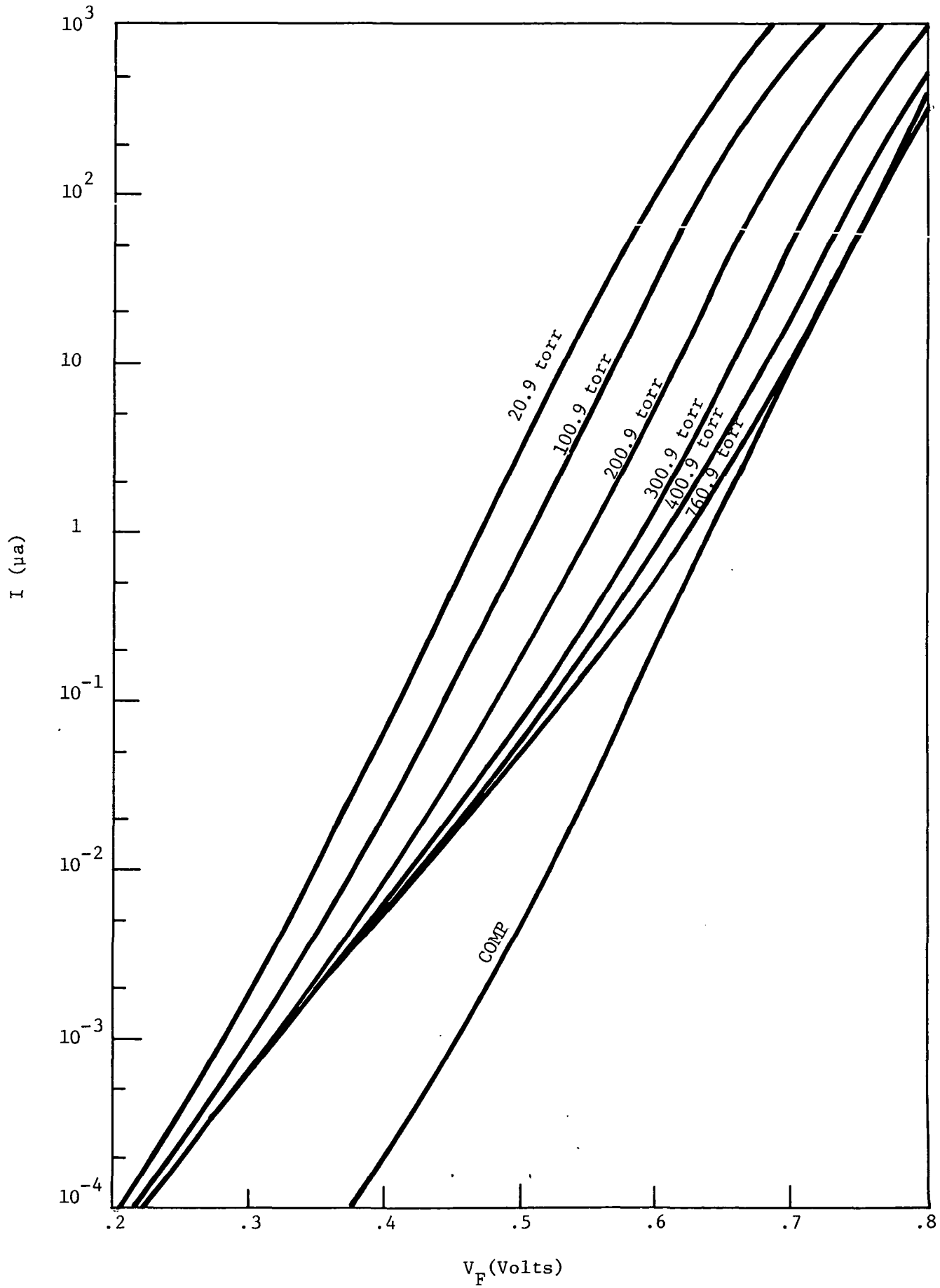


Figure 42. Log Current-Voltage Characteristics of Transducer 29-1

not ideal, these characteristics are useful as piezo junction diodes and fully justify their use in this research in place of the in-house planar mesas described in Part A.

Figure 43 shows additional measurements on transducer 29-1 in which forward current at fixed forward voltage (V_F = 0.6 v) is plotted against absolute pressure with temperature as a parameter. This display reveals:

1) the magnitude of the dead space for 29-1;

2) the temperature sensitivity of the characteristics; and

3) the presence of an undesirable hysteresis and/or instability.

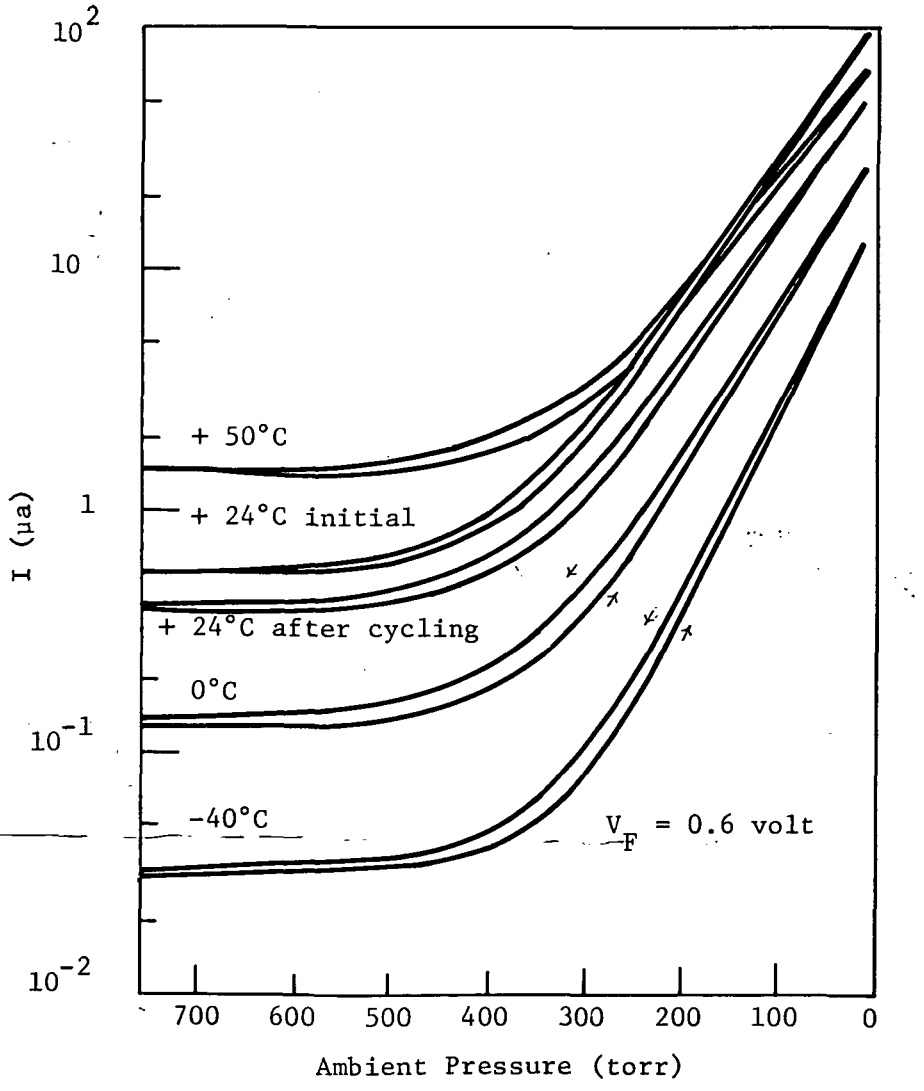


Figure 43. Pressure Sensitivity of Transducer 29-1

The dead space is caused by the separation between the planar mesa diode and the loading mesa of the diaphragm member that exists at an ambient pressure of 1 atmosphere. As the ambient absolute pressure decreases, the diaphragm relaxes and loads the planar mesa. For transducer 29-1 the loading becomes effective at about 500 torr. As the ambient pressure decreases further the load on the planar mesa increases further. The region of highest interest 10 torr < ambient pressure < 10^{-3} torr, is not shown in Fig. 43; such data have not yet been taken. Simple extrapolation of the plots in Fig. 43 indicate that a pressure change of 10^{-3} torr should cause at least a one namp change in forward current (current increase from say 100 μa to 100.001 μa). This value is most likely buried in the device noise and hence represents a useless output. Determining the smallest pressure change capable of producing acceptable signal to noise is a necessary measurement for complete evaluation.

The temperature dependence of the transducer follows roughly what would be expected from eq. 18 (p. 13, Part A). Equation 18 states that the forward current is proportional to three exponential terms [Ref. 6] (exp (qV/kT) >>1):

$$I_F = K \exp\left(\frac{qv}{kT}\right) \exp\left(-\frac{E_g}{kT}\right) \exp\left(\pm \frac{\Delta E_g(\text{eff})}{kT}\right) \tag{37}$$

the I_o factor of eq. 18 being replaced by the E_g exponential and the $\gamma(\sigma)$ factor by the effective change in bandgap induced by mechanical stress. The first two factors of eq (37) are characteristic of any p-n junction and reflect the dependence of the forward current upon forward bias and band gap respectively. For silicon Eg ~ 1.12 eV at room temperature so this factor dominates the forward current temperature behavior when the diode is held at a fixed bias of 0.6 volt as has been true in all evaluation of transducer 29-1.

From eq. 37,

$$dI_F = -K \frac{qV - E_g \pm \Delta E_g(\text{eff})}{kT} \exp\left(\frac{qV - E_g \pm \Delta E_g(\text{eff})}{kT}\right) dT,$$

or

$$\frac{dI_F}{I_F} = -\frac{qV - E_g \pm \Delta E_g(\text{eff})}{kT} \frac{dT}{T}. \tag{38}$$

For the unloaded diode ΔE_g(eff) equals 0 and, at V_F = 0.6 volt, the incremental percentage change in I_F, as calculated from eq. 38, is about 20 times the incremental percentage change in temperature in the vicinity of room temperature.

This general behavior is observed in the characteristics shown in Fig. 43. The forward current of the unloaded diode is the current measured for absolute pressure > 500 torr.

The I_F temperature dependence of the compensating diode should be similar to that of the unloaded planar mesa when both characteristics are dominated by the same type of currents such as low injection diffusion current (the preferred operating mode at $V_F = 0.6$ volt). Thus the I_F for a planar compensating diode should be represented by a constant current line in Fig. 43 which varies with temperature similarly to the high pressure current levels illustrated.

Loading of the planar mesa diode changes the value of I_F and also the relationship between changes in temperature and changes in I_F. The influence of mechanical stress is incorporated into the junction characteristics by the $\Delta E_g(\text{eff})$ factor. For silicon this factor is positive under compressive stress and increases the forward current the same as an increase in forward voltage. The effect of increasing stress becomes evident as the absolute pressure falls below 500 torr in Fig. 43, causing rapid increases in I_F as predicted by eqs. 18 and 37.

The stress sensitivity of the planar mesa diode depends upon the change of I_F with stress which, on a semi-log plot of current vs. $\Delta E_g(\text{eff})$, is given by:

$$\frac{d(\log I_F)}{d(\Delta E_g(\text{eff}))} \equiv \log e \quad \frac{d(\ln I_F)}{d(\Delta E_g(\text{eff}))} = \frac{0.4343K}{kT} \tag{39}$$

The stress level in the planar mesa diode is directly proportional to the pressure differential across the diaphragm which is the abscissa in Fig. 43. While the band gap change $\Delta E_g(\text{eff})$ does not depend linearly on stress, the temperature dependence of the slope of I_F with pressure differential shows the general qualitative relationship indicated by eq. 39. The slope varies more as $T^{-1.5}$ than T^{-1}. No provision for compensating this temperature dependence exists in the present design; only the temperature dependence of the unloaded current can be compensated by the compensating diodes.

Of more interest and concern than the temperature dependence of the sensitivity of the planar mesa diode (which is expected and predictable from design equations) are the instabilities evident in all curves of Fig. 43. Two types of instabilities exist:

1) the standard hysteresis loop in which the characteristics for increasing pressure are not the same as those for decreasing pressure; and

2) the drift of the no-load current following pressure cycling, or a zero drift.

Temperature is not the cause of the hysteresis as can be seen by the display of Fig. 44. In making this plot the procedure was to trace out the falling pressure part of the curve as usual but then allow the transducer to remain at low pressure without power for 50 min. The pressure was slowly increased again but no power applied until the ambient pressure was nearly 460 torr. The hysteresis loop remains even though very low power dissipation occurs and the load is removed completely a few seconds following the reapplication of transducer power. As is evident in Fig. 44 the zero load current level differs from its original value. Although not apparent in Fig. 44, the zero load current will slowly drift back to its original starting value in about 10 min.

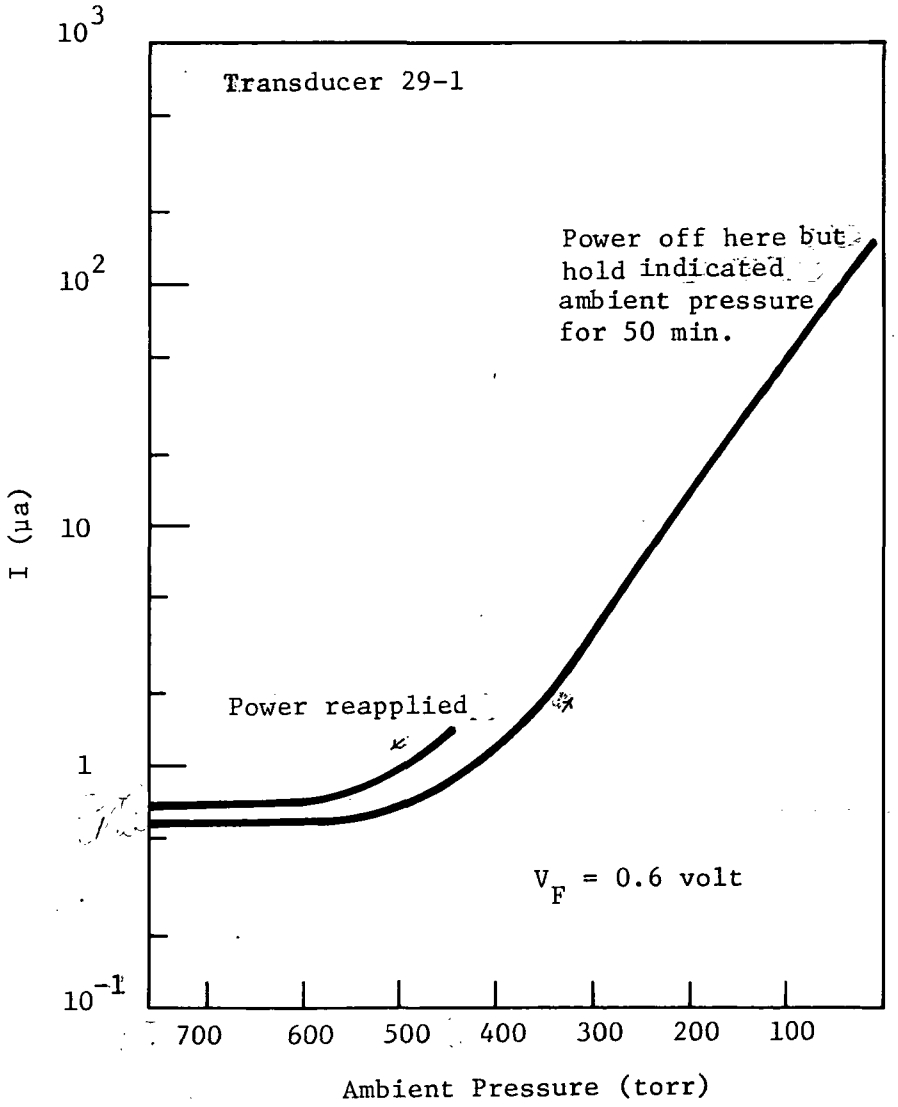


Figure 44. Evidence for hysteresis in the absence of temperature effects because of power dissipation

Two sources for the instabilities are possible:

1) mechanical creep and relaxation in the housing;

2) surface ion effects.

Mechanical creep is an old familiar nemesis for piezojunction transducers. Minimization of this effect was the prime reason for making both the housing and the loading surface of this present transducer out of silicon--the mechanical properties of silicon are superior to those of all other readily available materials. The present package does have glass seals but these seals extend over large areas surrounding the cavity and experience stress levels far less than those exerted on the loaded planar mesa. Piezoresistive diaphragms have been built and housed in similar diaphragm mountings without showing any creep effects. Stress levels in the package should not exceed 2-3 x 10^{10} N/cm^2 (2-3 x 10^9 dynes/cm^2).

Mechanical creep cannot be ruled out, however, because of the present variability in the quality of the electrostatic silicon-to-silicon seal. Some attempts are successful and others are not when evaluated by the most obvious measures--the seal is hermetic or not, the active element adheres to the diaphragm or it doesn't. Among those second seals -- the active element member to the diaphragm -- that are pronounced successful there is much room for variability. Under load one marginal seal might "give" a small amount -- bend elastically, for example, if attached only on one side -- and recover when unloaded. No good check now exists by which the second seal can be evaluated. Some are undoubtedly superior than others and hence, if mechanical properties of the seal are responsible for device instability, some transducers should exhibit instability and others not. This finding is the case as will be illustrated by the behavior of transducer 8-7 (to be discussed next).

A second source of transducer instability could be surface ion effects. Such effects should also be highly variable and unpredictable. They are also compatible with the time constants associated with the observed instability and would be expected to remain after the planar mesa is unloaded, as is observed in Fig. 43. At pressures greater than 500 torr, the planar mesa is unloaded unless gross distortions in the structural members occur. These are unlikely because the current-pressure curve repeats itself quite closely with respect to loading threshold on a day to day basis and shows good repeatibility in sensitivity. Drift or hysteresis in the properties of an unloaded planar mesa diode is compatible with temporary shifts in surface properties brought about by applied bias, contamination or both.

When operated at a forward bias of 0.6 volt, transducer 29-1 exhibits significant non-ideal current, most likely of surface origin, as is evident from the log I-V characteristics of Fig. 42. The difference between the compensating diode curve and the unloaded planar mesa (the 760 torr curve) is quite pronounced at 0.6 volt and is most likely due to enhanced surface current components associated with the planar mesa structure. If surface

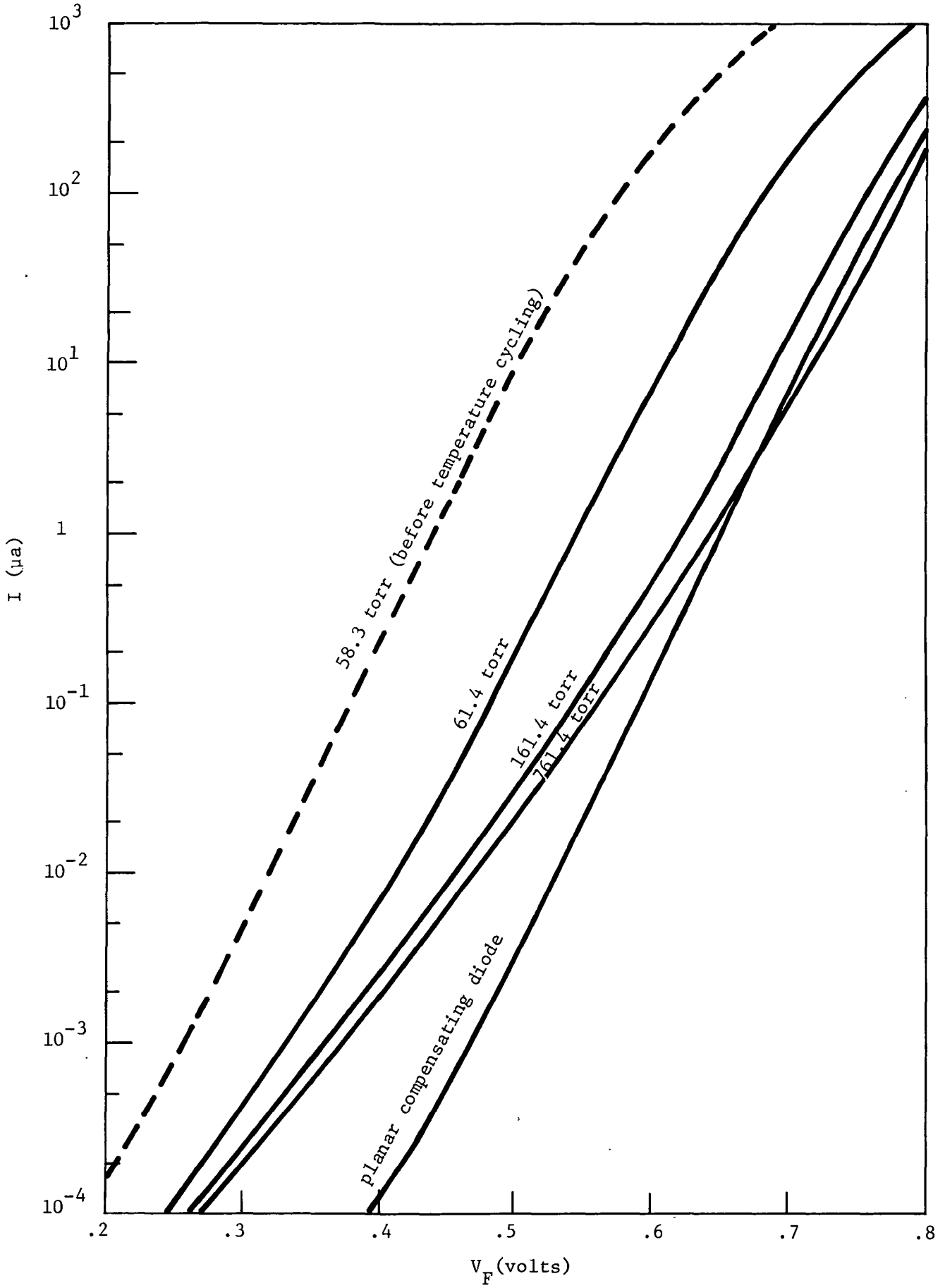


Figure 45. Log Current-Voltage Characteristics of Transducer 8-7

effects are causing the observed instabilities, an immediate solution is to operate at higher forward bias, say 0.7 volts. From Fig. 42, the difference between the planar mesa current and the compensating diode current is much reduced so that surface currents are less important at this bias. Measurements at 0.7 volt have not been made on 29-1.

Transducer 8-7

Figure 45 shows the log current vs voltage characteristics for transducer 8-7 at various ambient pressures; Fig. 46 is a plot of log current vs ambient pressure for room temperature operation. The dashed curve in both figures represents properties observed before cycling to

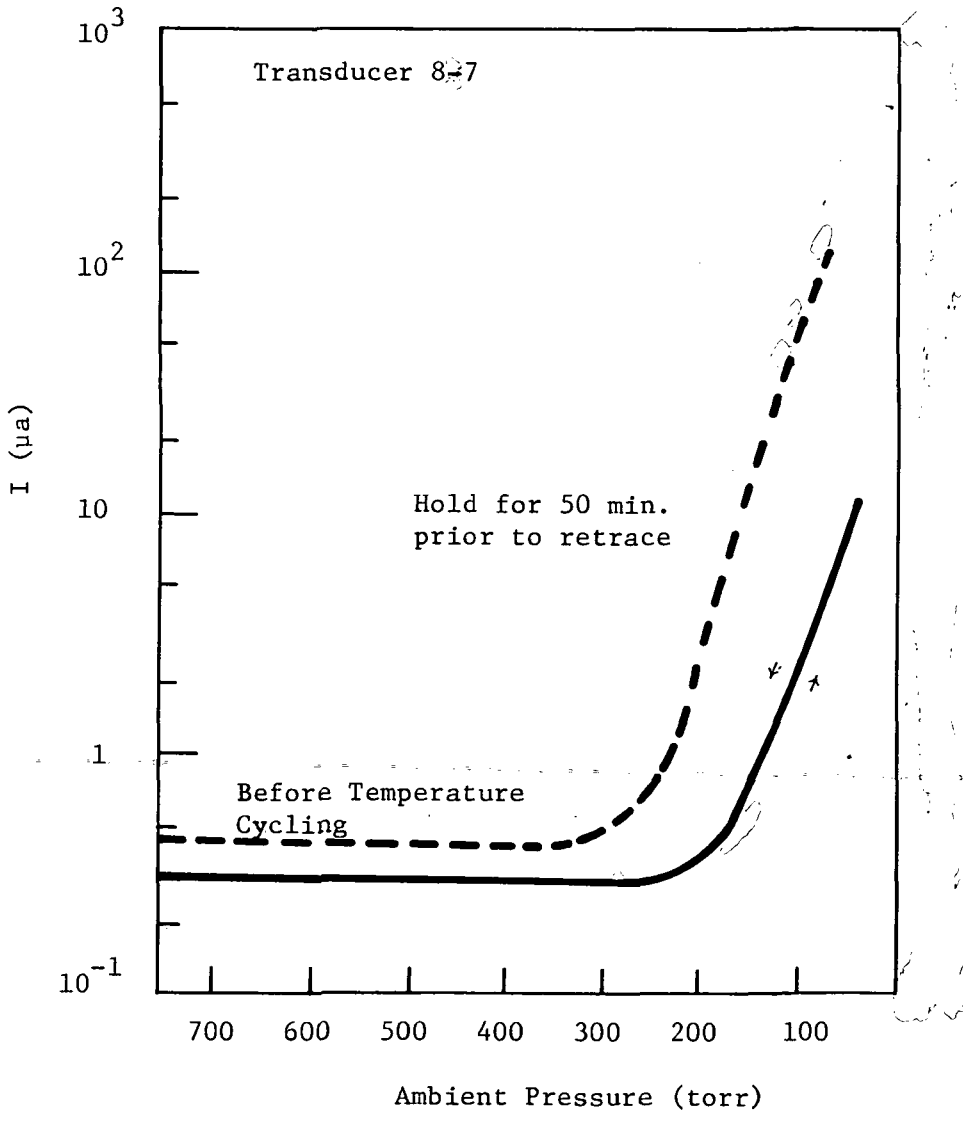


Figure 46. Pressure Sensitivity of Transducer 8-7

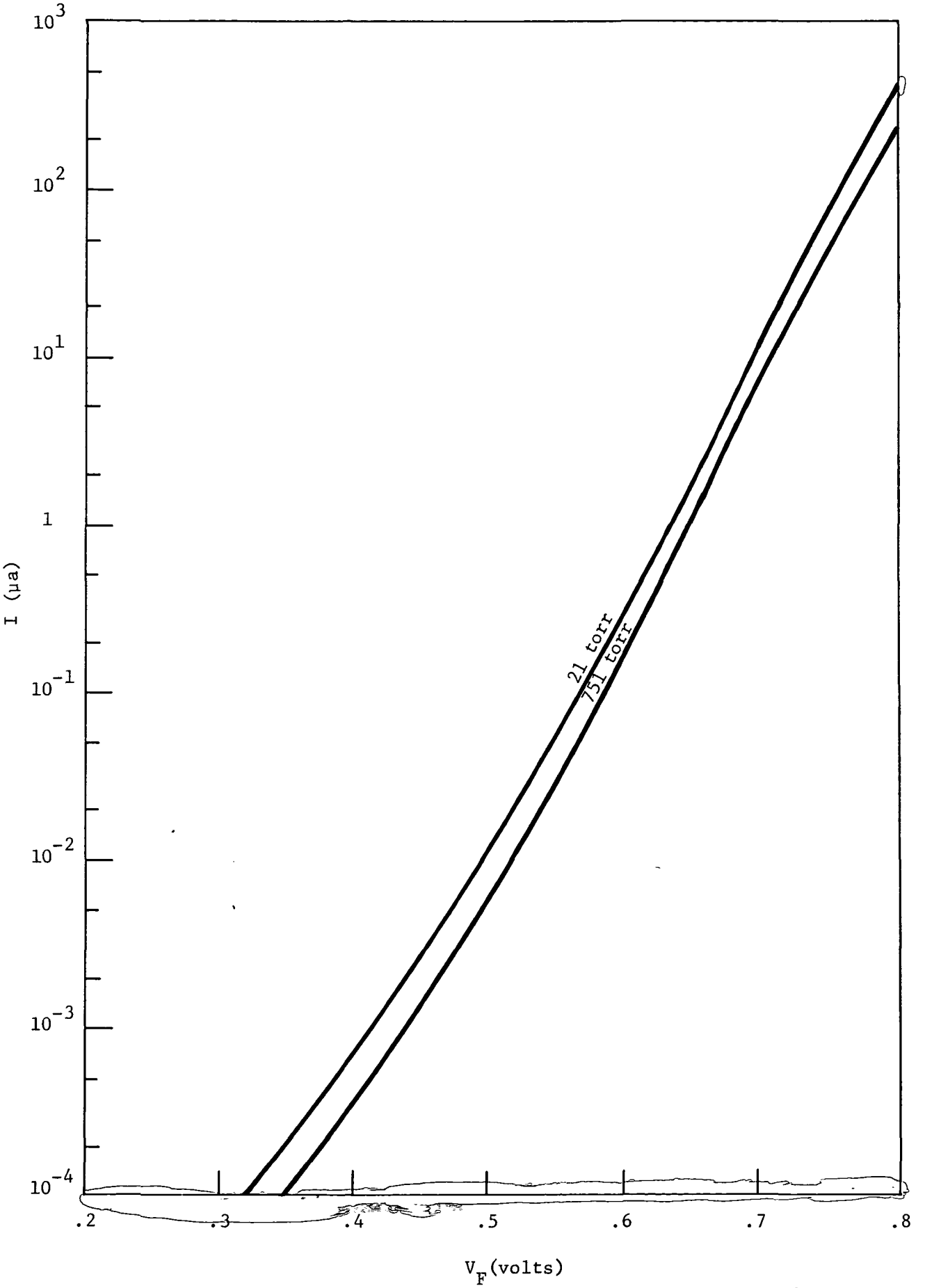


Figure 47. Log Current-Voltage Characteristics of Transducer 10-150

-40°C for test. The significant point to be made is that the low temperature testing caused irreversible changes in the transducer properties as evident from the altered dead space following the low temperature excursion. Such a change is consistent with altered mechanical properties of the second electrostatic seal. For example, if the low temperature cycling caused a partial seal rupture the net effect might be to simply increase the spacing between the planar mesa diode and the loading mesa of the diaphragm. Such an increase would produce the modified transducer properties observed

Rupture of the first seal would destroy transducer operation altogether. Since the transducer still operates, this possibility is ruled out.

In spite of this mysterious change in properties, the transducer does exhibit a freedom from hysteresis not seen in transducer 29-1. This conclusion applies both before and after the testing at -40°C, except that the unloaded current has changed. The difference in current at 760 torr in Fig. 46 is not just a convenient displacement for clarity but represents a change in the 0.6 volt zero load current.

As evident in Fig. 45, the unloaded planar mesa diode exhibits some departure from ideal diode behavior at a forward bias of 0.6 volt but not as much as did the planar mesa diode of transducer 29-1 (Fig. 42). Surface effects should be reduced in magnitude for transducer 8-7 (compared with transducer 29-1), although not eliminated.

Transducer 10-15

The third transducer tested was 10-15 which was a low sensitivity unit as illustrated in Figs. 47 and 48. The log current vs pressure curve (Fig. 48) displays significant hysteresis at room temperature. No temperature cycling was carried out on this unit.

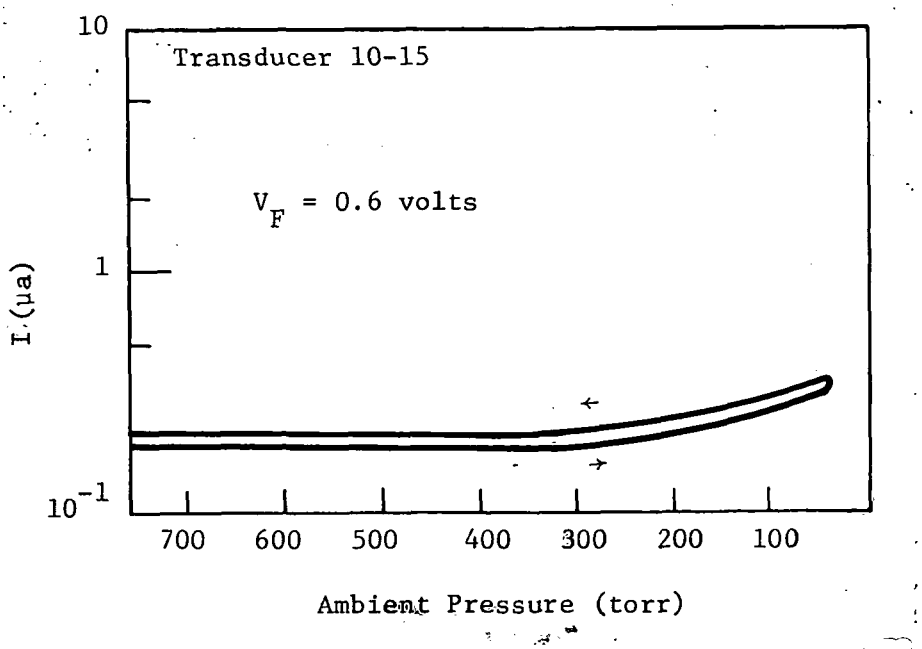


Figure 48. Pressure Sensitivity of Transducer 10-15

SECTION VI

CONCLUSIONS AND RECOMMENDATIONS

The modified transducer fabrication cycle in which a Pyrex cavity is substituted for the Pyrex coated silicon cavity leads to a higher yield process than the initial all silicon process. This change is regarded as an expedient only and was adopted in order to generate transducer test data before program termination. Development of techniques for depositing suitable glass layers for electrostatic sealing should be a first priority task for any future work to develop this transducer concept.

Limited transducer evaluation showed that the units could still exhibit undesired hysteresis and instability, although such shortcomings were reduced in magnitude over all previous piezojunction transduce concepts developed by RTI [Refs. 1, 2, 9, 11, 12]. Certain transducers were much freer from these effects than others; improved control over the processing should make such transducers the rule.

Evaluation of the transducers was not carried out at the low pressures (10 torr to 10^{-3} torr) of most interest. Certain of the units fabricated merit checking in this pressure range in order to define the lowest pressure at which adequate signal to noise can be generated.

The piezojunction technique continues to look promising for the fabrication of a transducer with good sensitivity at low pressure and with wide dynamic range. A completely satisfactory transducer has not yet been produced but the output of this project is closer to the goal than any previous structure. Among the remaining problems, in addition to the electrostatic sealing technique, are:

1) Control of the surface properties of the planar mesa diode;

2) Surface passivation;

3) Control of housing dimensions; and

4) Temperature compensation of the piezojunction effect.

The planar mesa diodes used in this project were fabricated by a commercial semiconductor manufacturer. These planar mesa diodes always exhibited greater recombination currents (most likely of surface origin) than did the adjacent planar compensating diodes surrounding them. The present units operated in the open atmosphere without any passivation other than thermal oxide. Additional surface preparation and passivating layers, such as those of silicon nitride, would be desirable in a production version.

Other features that would have to be improved for significant market p penetration include the assembly scheme and the circuit design. The present assembly does not allow control of the dead space beyond that which accompanies the tolerances in transducer assembly. What is needed is a scheme whereby the loading threshold can be preset before or during the final electrostatic seal. This capability plus a temperature compensating feature for the readout would make the unit of broad value. The unstressed diode of the present design compensates only the no-load current of the planar mesa diode. The bandgap changes induced by mechanical stress are also temperature dependent, making the load response of the planar mesa temperature dependent in an uncompensated mode at present.

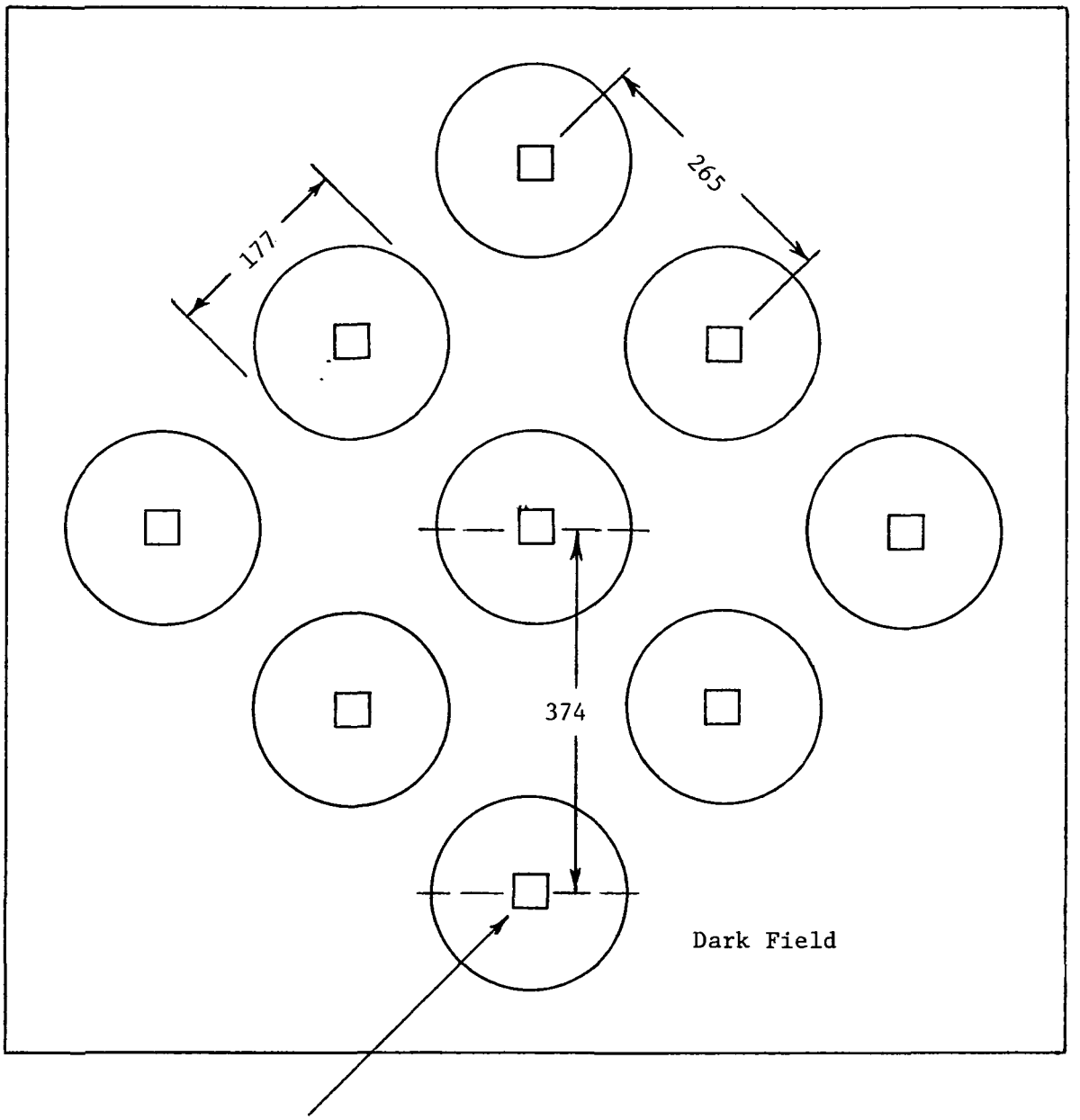
APPENDIX A

CAPSULE DIODE MASK-SET (PART A)

This appendix includes a detailed description of the mask-set used for fabricating the planar-mesa, capsule diode. Other mask-sets were used early in the program, but the set described herein represent the final design used in this investigation. Several improvements are possible with modifications in the mask-set, and these are discussed in Section 3 of this report. Delivery delays experienced in obtaining mask-sets were prohibitive for reflecting these improvements in this program.

Figures A-1 and A-2 illustrate the 3 x 3 and 2 x 2 diode arrays, respectively. Figures A-3 through A-6 illustrate the detail structure of the diode repeated in each circle of both the 3 x 3 and 2 x 2 arrays. For illustrative purposes, the mask-set will be described using the 2 x 2 array of Fig. A-1. This mask provides for etching the diaphragm, leaving a mesa structure in the center of each circle. Mask B (Fig. A-3) is the junction diffusion mask, an n-diffusion on a p-wafer. Mask C (Fig. A-4) provides for a n^+ contact diffusion when the processing is being done on a n-type substrate. Mask D (Fig. A-5) opens windows for metallization contacts to the substrate and the diffused diode region, and Mask E (Fig. A-6) is the metallization mask. Fig. A-7 is an enlargement of the center portion of Mask E showing additional detail.

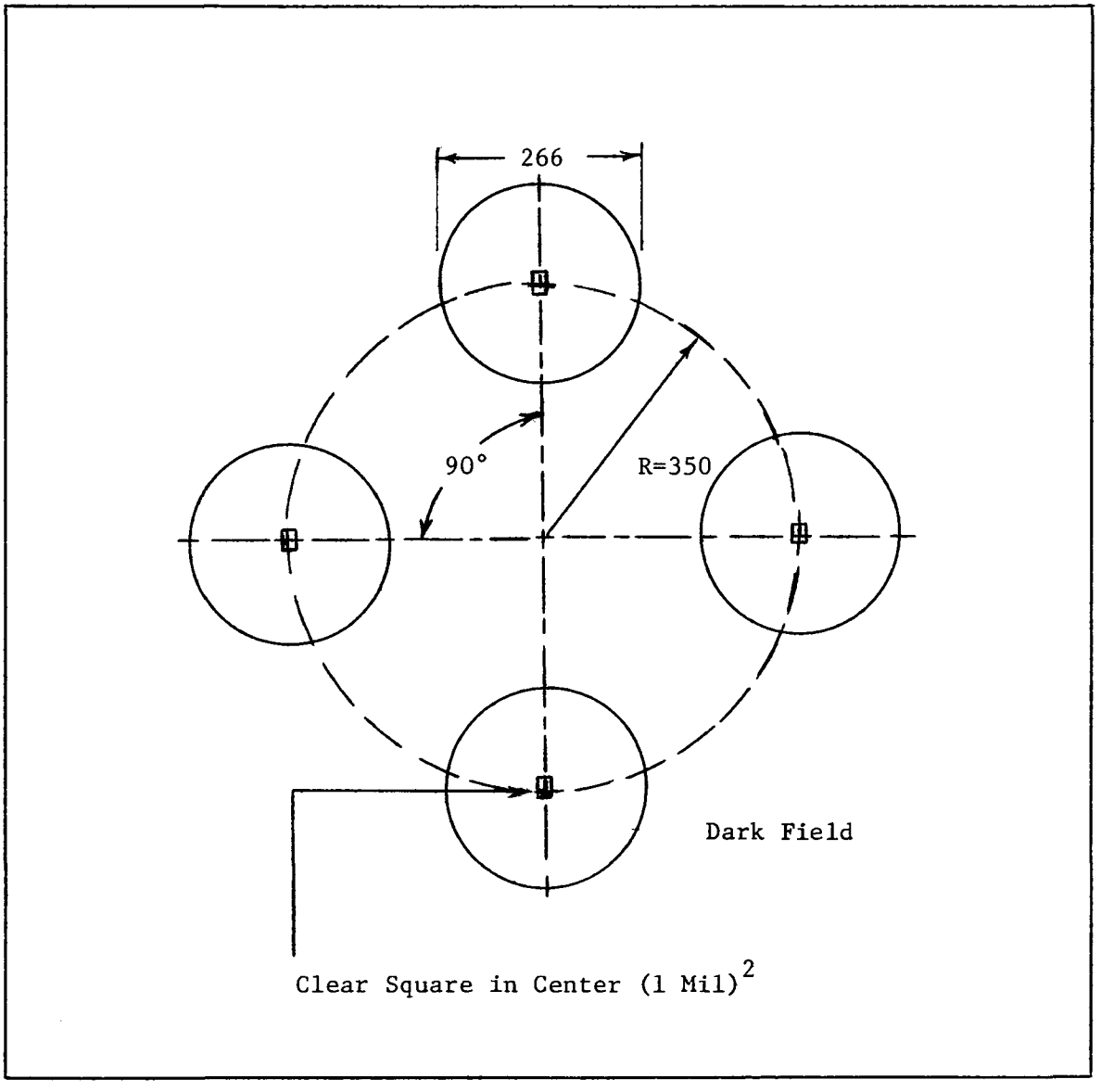
The center point of each Mask B through E aligns with all other centers. Dark and clear fields are identified on each figure. Fig. A-8 is a complete drawing illustrating the alignment of all the masks.



Clear Square in Center (1 Mil)^2

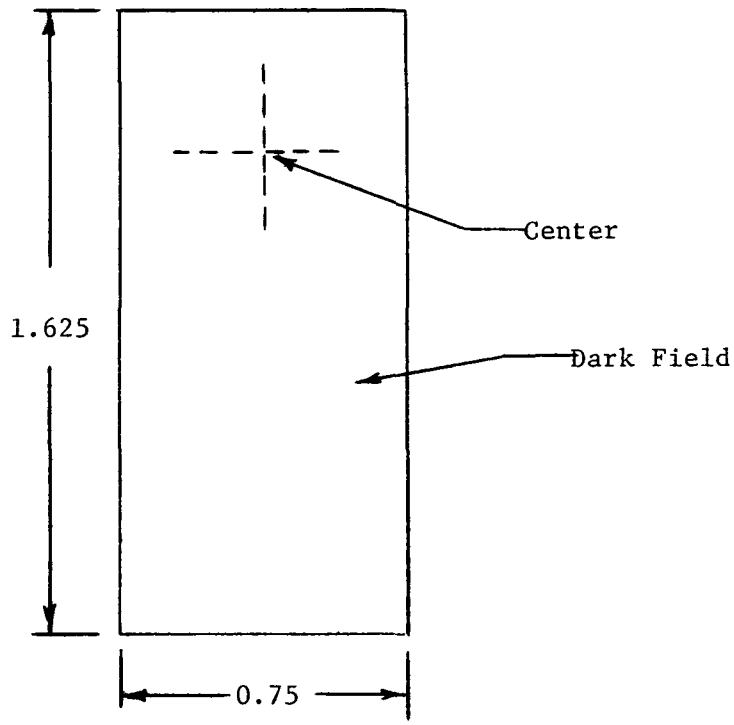
Dimensions Shown in Mils (Not to Scale)

Fig. A-1. Mask 1-A



All Dimensions are in Mils (Not to Scale)

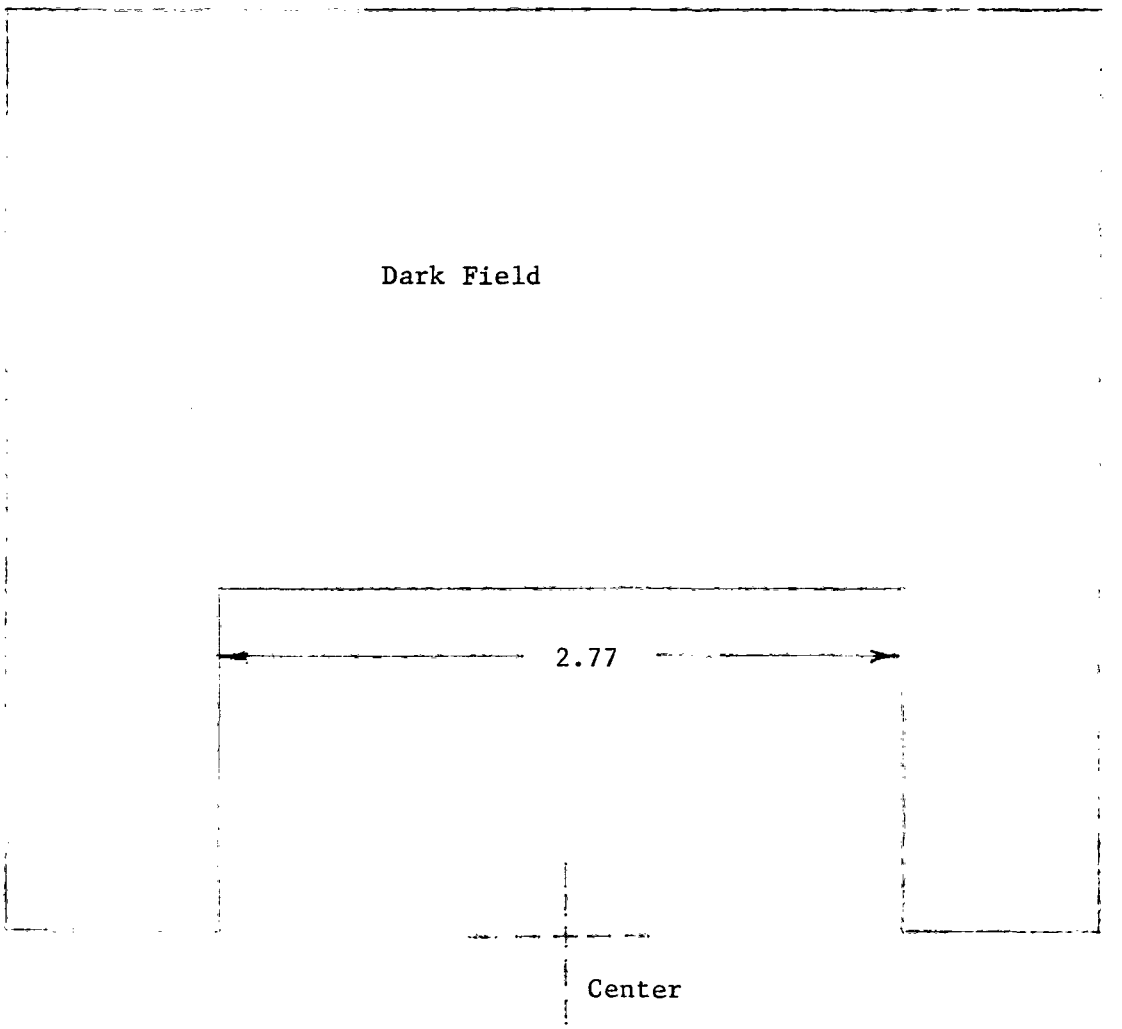
Fig. A-2. Mask A



Scale 2" = 1 Mil

All Dimensions in Mils

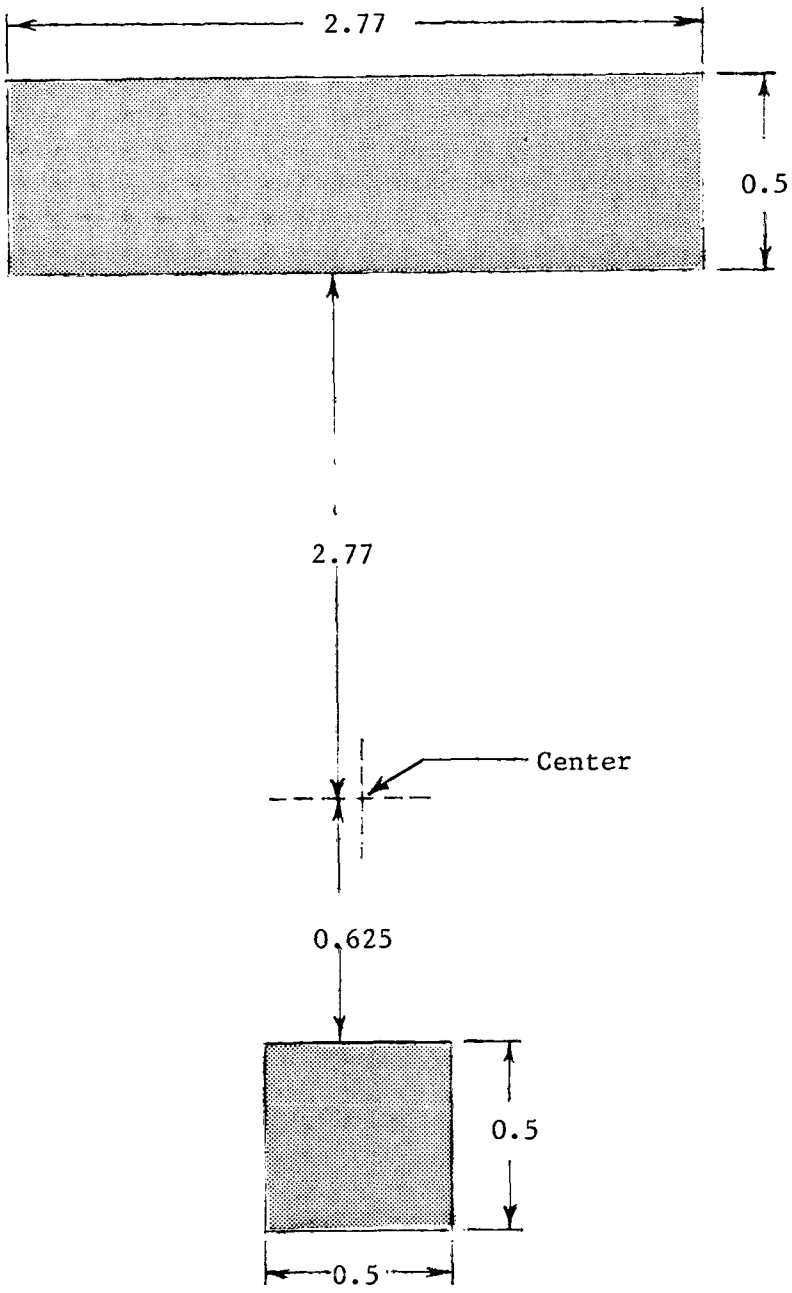
Fig. A-3. Mask B



Scale 2" = 1 Mil

All Dimensions in Mils

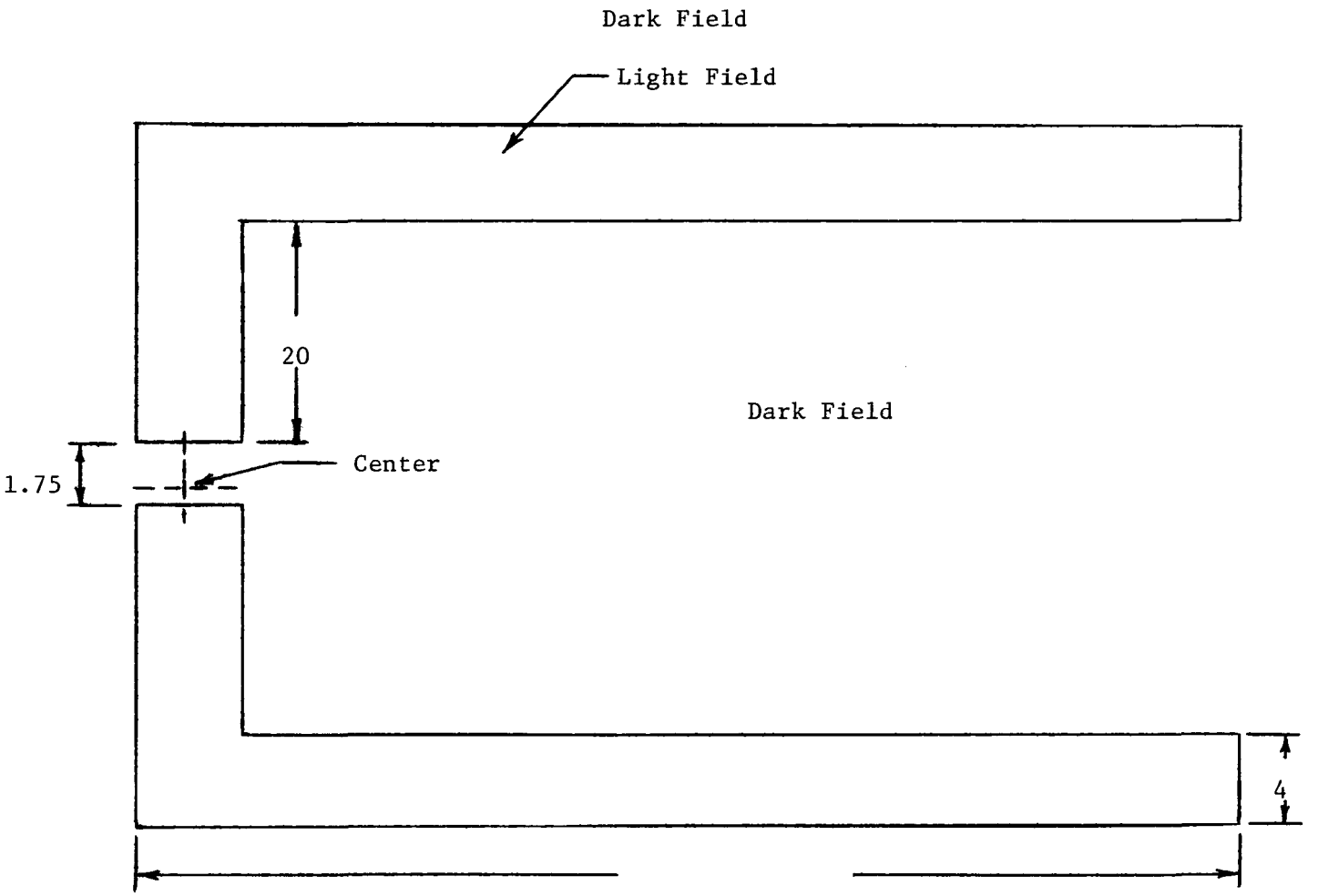
Fig. A-4. Mask C



Scale 2" = 1 Mil

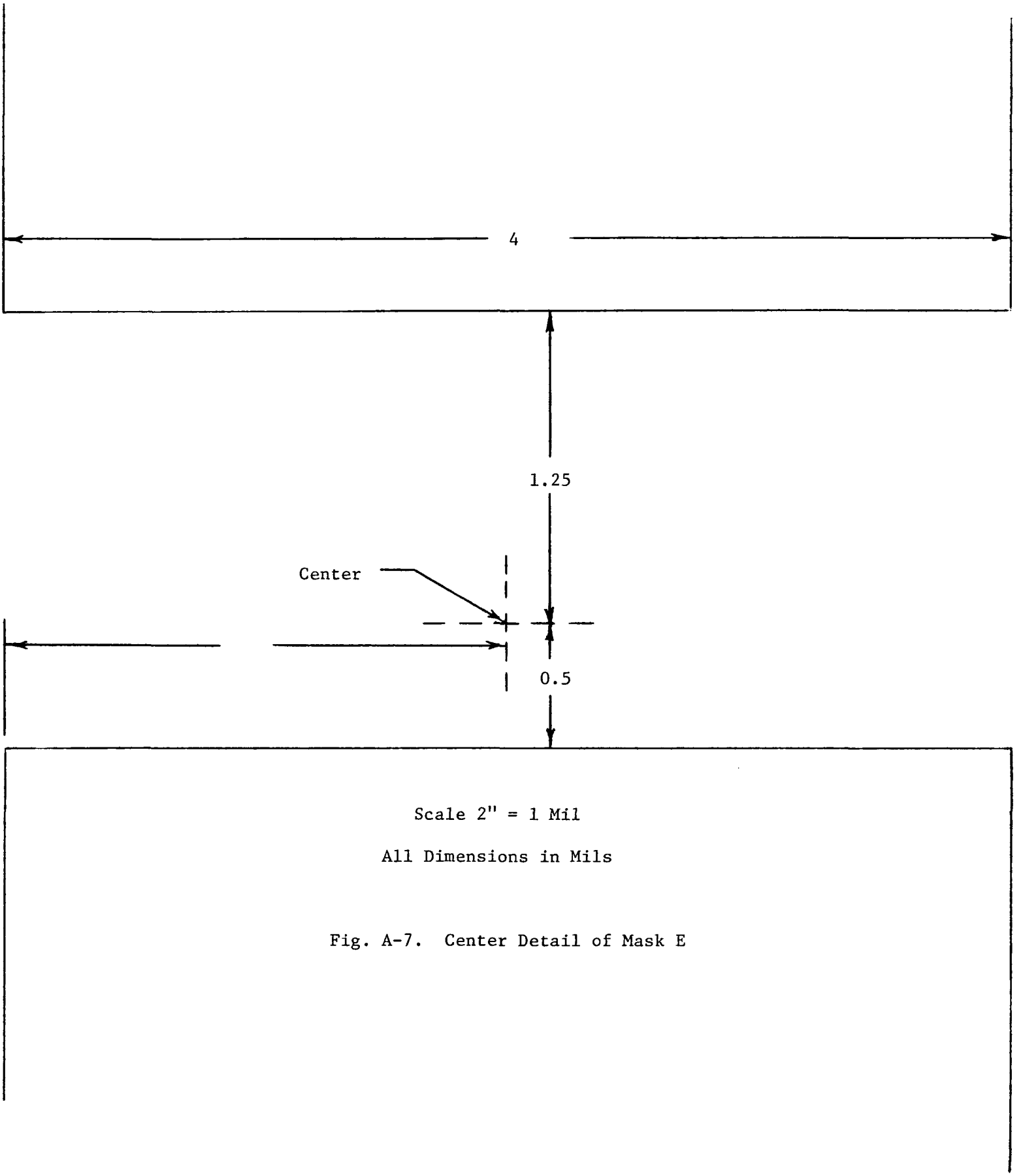
All Dimensions in Mils

Fig. A-5. Mask D



All Dimensions in Mils (Not to Scale)

Fig. A-6. Mask E



Scale 2" = 1 Mil

All Dimensions in Mils

Fig. A-7. Center Detail of Mask E

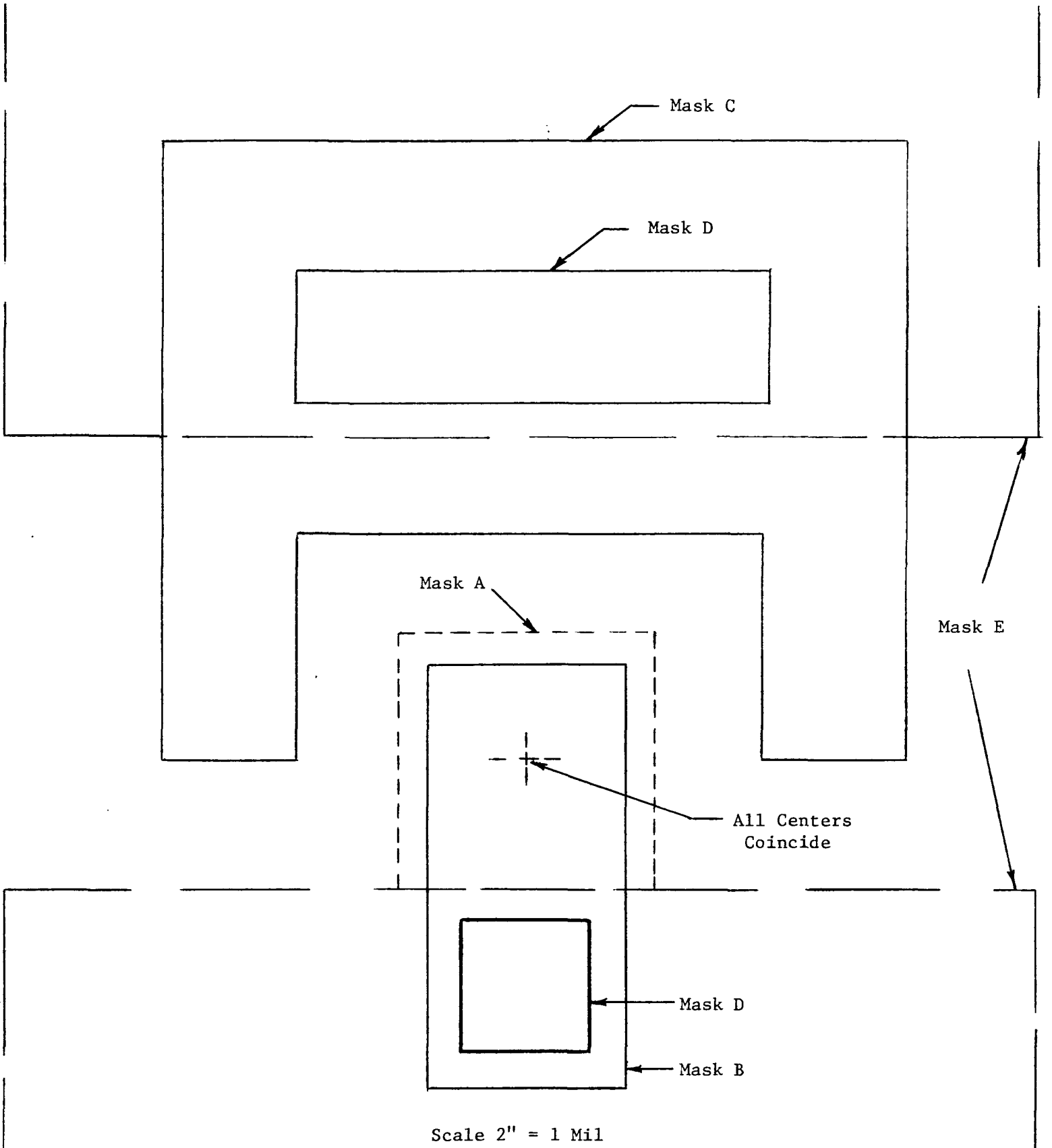


Fig. A-8. Composite Drawing of Complete Mask Set

APPENDIX B

SEMICONDUCTOR PROCESSING PROCEDURES

The following is a detailed, step-by-step description of the processing procedures that yielded the best results during this program. The starting material was 1-0-0, 0.5 Ω-cm, p-type silicon wafers approximately 1 1/4" in diameter and 0.008" thick. The p+ diffusion included in the process was to prevent inversion layers from forming at the surface of the wafer. The masks used are described in Appendix A.

1) Oxidation: oxidize wafers (5 min dry O_2, 65 min steam, 5 min dry O_2) at 1100°C, producing a 7000 Å oxide.

2) Apply KPR-2 (preheat wafer for 2 min at 1100°C, if allowed to cool after oxidation), one coat.

3) Bake 15 minutes at 85°C.

4) Mask: Mask A - expose 1 min (0.8 mil square oxide for mesa (align flat 45° to mask orientation))

5) Develop 3 min in TCE. Dip in and spray with acetone.

6) Paint KPR2 over as much of the oxide area as possible.

7) Bake 15 min at 160°C.

8) Etch wafers for 12 min in a solution of 90% ammonium fluoride (40% soln) and 10% HF. Rinse in flowing DI H_2O and blow dry with N_2.

9) Heat sulfuric acid before inserting wafer to remove KRP. Boil for 30 min, rinse in flowing DI H_2O and blow dry.

10) Apply black wax to back of wafers.

11) Silicon etch: 60 ml nitric acid, 10 ml acetic acid, 8 ml HF. Use 15 ml plastic beaker with hose inlet at bottom for nitrogen flow. Dip wafer in nitric acid for 2 min. Pull wafer from nitric acid and quickly place in etch solution for 57 sec with nitrogen flowing in beaker. After 57 sec (use glove), flood beaker with water and rinse out etching solution. Rinse in DI H_2O (beaker and wafer). Pull wafer from beaker and dry off in N_2. Hold hose up so as not to let water run out. Pour H_2O out of beaker and spray wafer with acetone and dry. At this point the devices are 1/2 mil flat top mesa; all of the oxide is etched off.

12) Boil in TCE to remove wax.

13) Dip in HF 2 min to remove any remaining oxide from top of mesa. This also removes the large area of oxide. Rinse in DI H_2O and warm Transene.

14) Round off edges of cavity and mesa with silicon etch as in Step 11 above. Etch for 8 sec. (Scribe identification letter in wafer just above flat.)

15) Heat in sulfuric acid for 15 min, nitric acid for 10 min, rinse in DI H_2O and warm Transene.

16) P-type diffusion of wafer: 40 ppm, B_2H_6, 1000°C, 20 min; N_2 flow = 3800 cc/min; O_2 flow = 50 cc/min; B_2H_6 flow (1000 ppm tank mixture) = 160 cc/min.

17) Remove Borate Glass in 10% HF for 30 sec: (100 ml beaker - 5 ml HF, 45 ml DI H_2O). Rinse in DI H_2O and warm Transene.

18) Oxidation in Diborane Furnace: 1150°C, 30 min, steam only. 5500 Å oxide.

19) Apply KPR2 after 2 min at 1100°C. One coat.

20) Bake 15 min at 85°C.

21) Mask: Mask B - expose 8 sec (diffusion mask for diode - "n" diffusion on "p" wafer - 3/4 mil × 1.66 mil).

22) Develop 3 min in TCE. Dip in and spray with acetone.

23) Apply KPR2. Paint on KPR2 under microscope. Wet brush with KPR2 and push resist up to unit within two to three mils. Apply resist only on "n" diffused side (lower side next to flat). Carry resist outside the cavity. Bake 5 min at 85°C. Coat entire back side with KPR2.

24) Bake 15 min at 160°C.

25) Etch wafers for 8-1/2 min in a solution of 90% ammonium fluoride (40% solution) and 10% HF. Rinse in flowing DI H_2O and blow off.

26) Heat sulfuric acid before inserting wafer to remove KPR. Boil for 30 min. Rinse in flowing DI H_2O and blow off.

27) Heat in nitric acid for 10 min. Rinse in DI H_2O and Transene.

28) N-type diffusion of wafer: 250 ppm, pH_3, 1100°C, 30 min. O_2 flow = 80 cc/min; N_2 flow = 2920 cc/min; pH_3 flow (980 ppm tank mixture) = 1000 cc/min.

29) Remove phosphorus glass in 10% HF for 30 sec: 100 ml beaker - 5 ml HF, 45 ml DI H_2O. Rinse in DI H_2O; warm Transene.

30) Oxidation in phosphine furnace: 1100°C. 50 min, steam only. Load in steam, remove in steam. ~6100 Å oxide.

31) Coat with KPR2 after 2 min at 1100°C. One coat.

32) Bake 15 min at 85°C.

33) Mask: Mask D - expose 20 sec. Contact mask ("n" diffused region and "p" substrate) 1/2 × 1/2 mil "n" contact.

34) Develop 3 min in TCE. Dip in and spray with acetone.

35) Apply KPR2. Paint on KPR2 under microscope. Wet brush with KPR2 and push resist up to unit within two to three mils. Apply resist only on "n" diffused side (lower side next to flat). Carry resist outside the cavity. Bake 5 min at 85°C. Coat entire back side with KPR2.

36) Bake 15 min at 160°C.

37) Etch wafer for 12 min in a solution of 90% ammonium fluoride (40% solution) and 10% HF. Rinse in flowing DI H_2O and blow off.

38) Heat sulfuric acid before inserting wafer to remove KPR.

39) Dip in 5% HF for 5 sec. Rinse in DI H_2O and Transene.

40) Evaporate aluminum on front surface in CVC unit. Preheat substrate 10 min, ~200°C.

41) Coat with KPR2 after 5 min at 160°C. One coat.

42) Bake 15 min at 85°C (no vacuum).

43) Mask: Mask E - expose 1 min. (Al mask for contact strips, 4 mils wide.)

44) Develop 3 min in TCE. Dip in and spray with acetone.

45) Bake 10 min at 160°C.

46) Apply black wax with wire to aluminum strips at points where they cross cavity edge. Bake 5 min at 85°C.

47) Aluminum Etch: 5 min for 500 Å, 20 parts phosphoric acid, 5 parts DI H_2O, 2 parts nitric acid. Rinse in warm DI H_2O and warm acetone; dry.

48) Remove KPR2: Resist strip J-153 concentrate used as follows:

Pour the concentrate in the lid of a glass petri dish. Insert the wafer in the J-153 and scrub lightly with a cotton swab. Remove wafer and rinse in xylene, TCE, acetone, and warm Transene; dry.

APPENDIX C

THE RELATIONSHIP OF STRESS TO STRAIN

Strain and stress are related through Hook's generalized law,

$$[e_{ij}] = [S_{ij}]\,[\sigma_{ij}]\ , \tag{C-1}$$

where

e_{ij} = strain components,

σ_{ij} = stress components, and

S_{ij} = stiffness coefficients for the crystal.

For the case of the cubic, silicon crystal, Hook's generalized law is (Ref. 5)

$$\begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \\ e_6 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} . \tag{C-2}$$

With respect to notation, e_1, e_2 and e_3 are the principal strains e_{xx}, e_{yy} and e_{zz}; e_4, e_5 and e_6 are the shear strains e_{yz}, e_{xz} and e_{xy}; and

$$e = e_1 + e_2 + e_3. \tag{C-3}$$

With a general stress applied to a crystal, it is possible to evaluate the principal (with respect to the crystal axes) and shear strains. The strain components resulting from a stress are necessary for calculating $\gamma_\nu(e)$. For a hydrostatic stress of magnitude T,

$$\sigma_1 = \sigma_2 = \sigma_3 = -T, \text{ and}$$
$$\sigma_4 = \sigma_5 = \sigma_6 = 0 . \qquad \text{(C-4)}$$

From Hook's Law, the strain components are computed as

$$e_1 = e_2 = e_3 = - (S_{11} + 2\ S_{12})\ T, \text{ and}$$
$$e_4 = e_5 = e_6 = 0. \qquad \text{(C-5)}$$

For a uniaxial [111] stress of magnitude T,

$$\sigma_1 = \sigma_2 = \sigma_3 = \sigma_4 = \sigma_5 = \sigma_6 = - T/3, \qquad \text{(C-6)}$$

$$e_1 = e_2 = e_3 = - T(S_{11} + 2\ S_{12})/3, \text{ and}$$
$$e_4 = e_5 = e_6 = - T\ S_{44}/3. \qquad \text{(C-7)}$$

For a uniaxial [011] stress of magnitude T,

$$\sigma_1 = 0,$$
$$\sigma_2 = \sigma_3 = - T/2 , \qquad \text{(C-8)}$$
$$\sigma_4 = - T/2,$$
$$\sigma_5 = \sigma_6 = 0 ,$$

$$e_1 = - S_{12} T ,$$

$$e_2 = e_3 = - T(S_{11} + S_{12})/2 ,$$

$$e_4 = - T S_{44}/2, \text{ and} \qquad \text{(C-9)}$$

$$e_5 = e_6 = 0 .$$

For a uniaxial [100] stress of magnitude T,

$$\sigma_1 = - T,$$

$$\sigma_2 = \sigma_3 = \sigma_4 = \sigma_5 = \sigma_6 = 0 , \qquad \text{(C-10)}$$

$$e_1 = - S_{11} T ,$$

$$e_2 = e_3 = - S_{12} T , \text{ and} \qquad \text{(C-11)}$$

$$e_4 = e_5 = e_6 = 0 .$$

In the preceding equations the applied stress, T, is positive when compressional, and negative when tensional (Ref. 5).

The stiffness coefficients of silicon, S_{ij}, of Eq. (C-2) are given by Mason (Ref. 14) as follows:

$$S_{11} = 0.768 \text{ cm}^2/10^{12} \text{ dynes},$$

$$S_{12} = - 0.214 \text{ cm}^2/10^{12} \text{ dynes, and}$$

$$S_{44} = 1.26 \text{ cm}^2/10^{12} \text{ dynes.}$$

Reprinted from JOURNAL OF THE ELECTROCHEMICAL SOCIETY
Vol. 119, No. 4, April 1972
Printed in U.S.A.

APPENDIX D

Low-Temperature Electrostatic Silicon-to-Silicon Seals Using Sputtered Borosilicate Glass

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The Mallory electrostatic sealing process (1, 2) is a method of anodically bonding two dissimilar materials together to form a strong, hermetic seal which involves little alteration in the shape, size, and dimensions of the members making up the joint. Previous applications have involved the sealing of a metal or semiconductor to an insulator, such as glass or ceramic. In this brief note we describe a method for sealing two silicon surfaces together by depositing a thin, borosilicate glass layer on one of the polished silicon members to be sealed. Our method for depositing the borosilicate glass layer is sputtering. Most likely the method is equally applicable with other deposition methods capable of similar control of film composition and thickness.

Experimental Technique

The surfaces of the silicon members to be sealed are polished by either mechanical, electrochemical, or high-quality chemical methods. These surfaces are cleaned and stripped of any residual oxide by immersion in concentrated hydrofluoric acid. The surfaces are then coated with sputtered borosilicate glass. We used an MRC-340 sputtering unit fitted with a 5 in. Corning 7740 ("Pyrex") borosilicate glass target. R-F sputtering was carried out in a 1% oxygen in argon atmosphere. Power levels varied between 150 and 800W. The critical property for satisfactory sealing is a minimum glass thickness of approximately 4 μm. Below this thickness the areas of satisfactory seal between the two silicon members are patchy and discontinuous. Substrate temperature during deposition was not controlled directly; the copper block upon which the silicon samples rested was either held at a temperature of about 50°C by water cooling or allowed to reach a temperature as high as 380°C when no water cooling was used. The sealing behavior of the sputtered film appeared insensitive to the deposition temperature over this span. No means of insuring good thermal contact between the silicon and the copper block was employed so that the temperature of the silicon samples themselves was most likely higher than that of the measured temperature of the copper block.

After sputtering the borosilicate glass layer, each coated silicon substrate was annealed, most often in steam, at a temperature between 500°-900°C. This steam annealing greatly improved yield during the subsequent sealing operation. The annealing temperature and ambient are not critical, but inclusion of some high-temperature heat cycle is required for satisfactory seals. Oxygen and nitrogen ambients during annealing were also used. Slightly higher yield during sealing seemed to be associated with the steam anneal.

To carry out the silicon-to-silicon electrostatic seal, a second polished silicon chip is placed on top of the first silicon member which is already coated with borosilicate glass. This second silicon member is polished by the same technique used to prepare the first surface. The two members are aligned in the desired orientation and held in position by a weight which is electrically conductive so as to serve as a top electrode as well as a pressure load. The combination is then heated on a graphite strip to a temperature of 450°-550°C. After the sandwich is stabilized at temperature, a slowly increasing d-c voltage is applied across the silicon-borosilicate glass-silicon sandwich, the uncoated silicon member being positively biased with respect to the glass-coated member. The primary control during sealing is total current flow which was limited to about 0.5 mA for these samples (corresponding to a current density of approximately 1 mA/cm^2). The voltage is advanced in steps as the current decreases with time. A maximum voltage of 50V is adequate for a satisfactory seal. After reaching the maximum voltage, the sandwich is left at temperature and voltage for 5 min. The substrate heater is then shut off so that the temperature of the sandwich can decrease to near room temperature before the voltage is turned off. This completes the sealing operation.

To evaluate the hermeticity of such a seal a number of silicon-to-silicon seals were prepared in which one silicon member of the silicon-borosilicate glass-silicon sandwich had a deep cavity etched part way through it. The second silicon member was then thinned to a total thickness of 0.025-0.1 mm (1-4 mils) and the sealing operation was carried out inside a vacuum chamber at a pressure of approximately 10^{-5} Torr. Upon completing the seal and removing the unit from within the chamber, atmospheric loading on the top, thin member of the sandwich produces a visible depression in the top member above the cavity in the bottom member, as illustrated in Fig. 1.

The top member of this particular unit is a piezoresistive silicon diaphragm with twelve junction isolated resistors ion implanted into its top surface. These resistors are positioned so that some are in tension and

* Electrochemical Society Active Member.
Key words: sealing, electrostatic sealing, hermetic, housing, packaging, silicon-to-silicon seals.

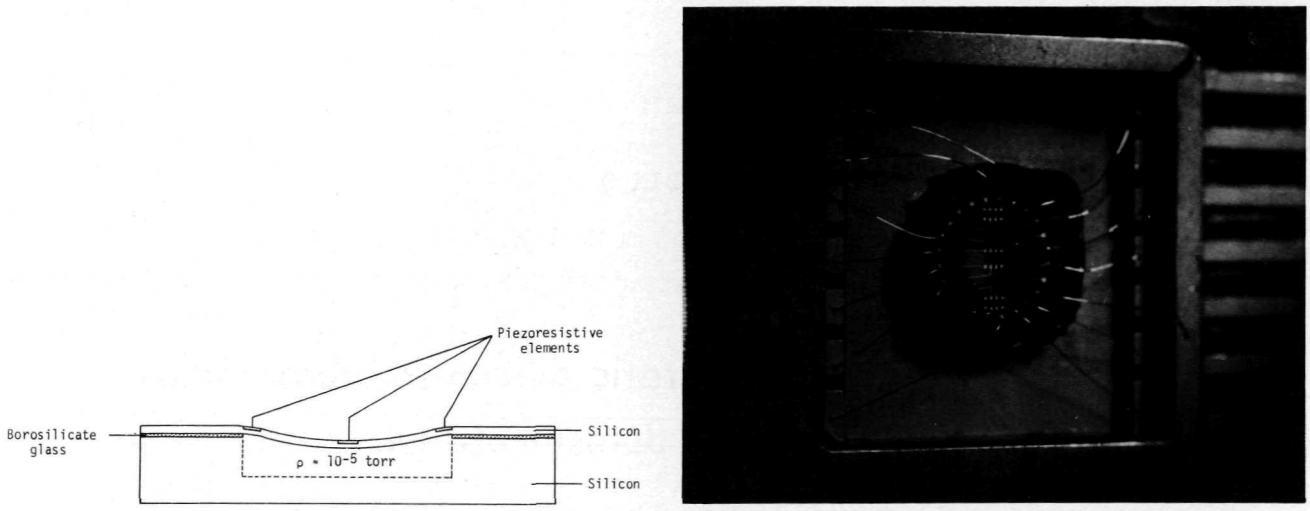

Fig. 1. Electrostatically sealed piezoresistive pressure transducer. (a, left) Sketch, (b, right) Photograph

others in compression because of the atmospheric pressure. When these resistors are externally connected in a Wheatstone bridge configuration, the output voltage of the bridge is a measure of the atmospheric pressure. The cavity diameter across which the thin silicon diaphragm is suspended is 2 mm in this illustration; the sealing area is a 1 mm ring surrounding the cavity. Reducing the ambient pressure surrounding the structure of Fig. 1b causes the dimple to disappear because the diaphragm is thereby unloaded.

Bottom views of similarly sealed units are shown in Fig. 2. The unit on the left is a silicon diaphragm electrostatically sealed to a borosilicate glass cavity. The cavity dimensions and position are clearly visible in this unit; the silicon unit on the right is identically shaped and has been sealed using the borosilicate glass methods described in this paper. These units are only one example of the application of this technique; both larger and smaller areas have been sealed. No effect associated with area has been identified. Current density during sealing has been held to $\lesssim 1$ mA/cm^2, but this current density is not optimum or anything more than an arbitrarily selected, convenient value.

An evacuated cavity such as that illustrated in Fig. 1 has been measured as essentially leak-free by helium leak-testing. Even after 63 thermal cycles between $+100°$ and $-40°$C, the unit showed no loss of dimple or measurable leak rate by helium leak-testing. To carry out the helium leak test, the unit was stored in a helium atmosphere for approximately 3 weeks at a pressure of 2×10^5 N/m^2 (2 atmospheres) of helium.

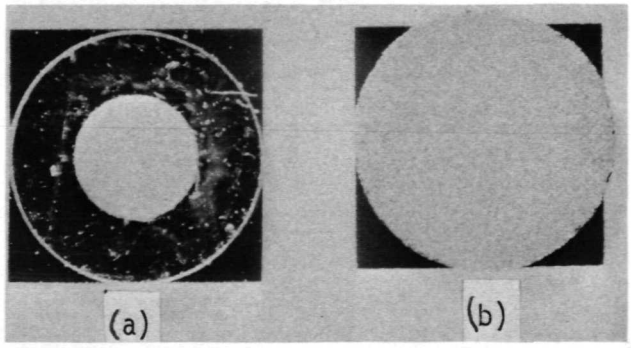

Fig. 2. Bottom view of electrostatically sealed piezoresistive pressure transducers. (a) Borosilicate glass cavity, (b) Silicon cavity.

The unit was then placed in the helium detection chamber in order to measure trace quantities of escaping helium. No traces of helium could be detected.

No other evaluation of the quality of this seal (such as tensile or shear tests) has been made; the thermal shock limits have not been determined. The value of the process is its compatibility with sealing to silicon device structures which have already been metallized with aluminum. Previous methods for housing silicon elements in silicon packages have involved higher temperature processes and have therefore required that metallization follow the sealing (3). Elimination of this restriction allows greater freedom in both device and package design.

Conclusion

A technique has been described for hermetically sealing silicon members to each other at a temperature $\lesssim 500°$C. The method involves no measurable deformation of the surfaces being sealed and hence is compatible with package designs of tight tolerance. The advantages of the all-silicon package are especially important for compensating the effect of temperature upon piezoresistive and piezojunction sensors. Since a low-pressure reference can be sealed between two members, the technique is compatible with the construction of absolute pressure transducers.

Acknowledgments

The sputtering apparatus employed in this work was made available to us by the Electrical Engineering Department at North Carolina State University, Raleigh, North Carolina, through the courtesy of Dr. M. A. Littlejohn. It is a pleasure to acknowledge helpful suggestions for this work from Drs. G. Wallis and D. Pomerantz of P. R. Mallory Company, Burlington, Massachusetts, and Drs. L. Maissel and W. Pliskin of IBM Corporation, East Fishkill, New York.

This work was sponsored by NASA, LRC, Hampton, Virginia 23365, under Contract NAS1-9005.

Manuscript submitted July 20, 1971; revised manuscript received Nov. 22, 1971.

Any discussion of this paper will appear in a Discussion Section to be published in the December 1972 JOURNAL.

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APPENDIX E

Solicitation Mailed to Potential Suppliers for the Fabrication of Pressure Transducer Parts, including an Outline of the Processing Steps and Sketches of the Photomasks to be Used (Part B).

ASSISTANCE FOR PRESSURE TRANSDUCER FABRICATION

This solicitation is for furnishing three silicon elements (1 active, 2 structural) to be used in constructing a piezojunction pressure transducer housed in an all-silicon package. The silicon used to make the active element of the transducer should come from the same ingot as that used to make the structural members. Shaping and processing of the structural members (named the cavity member and the diaphragm member) of the transducer will be done primarily by RTI using silicon wafers furnished by the supplier of the active element. Consequently, responders are requested to bid on furnishing 50 silicon wafers processed to yield the structure of the active member and 30 silicon slices each for fabrication of the cavity member and the diaphragm member. (Alternatively, RTI will furnish the silicon for all members. The key requirement is that all silicon be from the same source and preferably the same ingot.)

Photomask preparation can be one of two ways; RTI will either furnish the photomasks for the fabrication or will furnish sketches to which photomasks will be prepared. In the latter event the vendor will be asked to prepare photomasks to be used in processing the structural members. These photomasks will not actually be used by the vendor, but will be shipped to RTI along with the silicon. Each vendor is asked to specify in his response which option he is bidding on or to submit bids on both options.

SENSOR ASSEMBLY

The assembly steps for manufacturing this pressure transducer and the specifications for the silicon members are given in this section. The starting silicon is (100) p-type silicon doped to a resistivity of 0.02Ω cm. All three members of the package are made from the same ingot. Two thicknesses of wafers are required in quantities of 30 each. For making the cavity member, the finished surface thickness of the wafer is 23 mils ± 20%. One side of the wafer is mechanically polished to a flatness of one interference fringe and a parallelism of ± 2 μm. The bottom side of the wafer is flat. The silicon for fabricating the diaphragm member is finished on both sides to the same specifications as the polished surface of the cavity member. This wafer has a thickness of 3.8 mils to 4.2 mils.

The cavity is defined by mask 8 on the 20 mil thick silicon wafer. This wafer is subsequently etched and sawed along the boundaries also defined by the mask. This processing will be carried out by RTI. Furnishing the silicon and the photomasks for this construction, however, are optional parts of the procurement. Mask 9 outlines a layer to be deposited by RTI.

The diaphragm member of this silicon package is formed by a similar process in that mask 5 is used to define regions to be etched away from the thin silicon member and masks 6 and 7 define regions of deposited coatings. This processing will also be carried out at RTI; what is sought here are quotes on the silicon and the photomasks for this processing.

The third silicon member is that containing the active elements of the package. The finished wafer thickness should be at least 18 mils cut from the same ingot used to prepare the silicon slices for the structural members. One side of this wafer can be lapped, the other side is polished by processes compatible with planar technology. The two surfaces of the wafer should not deviate from parallelism by more than 1/2 mil across the diameter of the wafer.

Processing of the active member begins with an oxidation step which will subsequently be used to mask the silicon etch necessary for mesa formation. The oxide is patterned by contact printing with mask #1 which defines a 1 mil^2 mesa in the center of an etched cavity. The silicon etch is carried out to a depth of 6-8 μm leaving the mesa top approximately 1/3 to 1/2 mils across. Following etching, the oxide mask is stripped from the wafer and the entire surface is reoxidized to form a diffusion masking oxide. This oxide mask is defined by mask #2.

Following the n^+ -diffusion, which is a diffusion similar to that for an emitter for an npn transistor, contact holes are etched according to mask #3. In addition to opening contact windows, it also removes the oxide on the sealing surfaces of the outside support structure and in the scribing grooves.

Mask #4 defines the metallization pattern. These stripes are 2 mils wide and include redundant contacts to the cathode of the stress sensitive planar mesa as well as multiple contacts to the substrate.

Three options are visualized in responding to this request for procurement: (1) vendor supplies all silicon, all photomasks and the processing for the active member 2; (2) vendor supplies all silicon and the processing for the active member 1; RTI provides all photomasks; (3) RTI provides all silicon and photomasks; vendors supplies processing only for the active member 1. These options are based on the assumption that all silicon members come from the same source and ingot, and that the photomasks for all processing, regardless of where it is carried out,

should be prepared by the same organization at one shooting. If RTI supplies the silicon, it most likely will come from Monsanto; RTI furnished photomasks will be prepared by a commercial mask facility.

A minimum response to this requesttof procurement is the processing of the active member which contains the diode region of the transducer. Under option 3 above, RTI will agree to furnish photomasks and silicon. Furnishing the silicon will include the etching of the mesas required for this structure. Not included in the previous outline are methods for protecting the planar p-n junctions formed on the active member. Since this transducer is designed to operate in an open ambient (no hermetic seal), some means of protecting the planar p-n junction is desirable. A preferred method is an overcoat of silicon nitride. Other methods are acceptable. A method of protecting the junction should be specified in the response. Note that the photomask for this process has not been included in the previous discussion. If RTI furnishes the photomasks, instructions for preparing whatever photomasks are necessary to carry out the surface protection process must also be furnished with the quote so that conformity of the entire photomask set is assured.

PROCESSING STEPS

Processing steps for the structural members of the transducer are as follows (to be done by RTI):

1. Using Mask 8, etch cavity in wafer to be used for making cavity member.

2. Spuuter Pyrex on the wafer so etched.

3. Saw wafer into 0.25" x 0.25" squares.

4. Etch the silicon to make the diaphragm member according to Mask 5.

5. Sputter Pyrex and etch according to Mask 6.

6. Evaporate aluminum and etch according to Mask 7.

7. Saw wafer into 0.25" x 0.25" squares.

8. Seal the diaphragm member to the cavity member, using ceramic jig. Set the sealed combination aside to await processing of the active member.

Processing of the active member of the transducer proceeds as follows (steps 1-8 to be done by vendor; step 9 to be done by RTI):

1. Oxidize 0.02 Ω·p-type silicon to form a mask for the silicon etch.

2. Print Mask 1 for the mesa etch and etch to a depth of 6-8 m.

3. Strip off remaining oxide and reoxidize to form a mask for n^+ diffusion.

4. Print Mask 2 to define the regions for the n^+ diffusion.

5. Diffuse an n-type, emitter-like region; reoxidize and overcoat with thin silicon nitride layer for passivation.*

6. Open contact windows in the oxide over both the sealing land regions, the contact regions to the substrate and to the n^+ regions (Mask 3).

---

*optional; other methods capable of ensuring stable planar junction operation without a hermetic seal are acceptable.

7. Evaporate 10,000 A of aluminum.

8. Print and etch metallization mask (4).

---

9. Saw apart using the etched grooves as guidelines.

ASSEMBLY

This sequence describes the steps in joining the active member to the previously sealed vacuum reference combination (to be done at RTI):

1. Using the same fixture used to join the cavity and the diaphragm, place member from Step 9 above in position and electrostatically seal.

2. Remove the sealed unit and mount in type FH-90, 14 lead flat-pack (this mounting should be with a flexible sealant such as RTV or silver paste).

3. Wire bond gold leads from the exposed pads to the outer leads in each corner of the flat pack. This utilizes at most 12 of the 14 leads on the FH-90. Unit is ready for test and evaluation.

MASK DIRECTIONS

Nine separate masks are required. These nine masks are to be used in processing three separate wafers. Masks 1 thru 4 are for the active element and consist of the following:

1. Mesa mask 1 consists of a step and repeated cell as shown in the drawing. The step and repeat is on 0.260" centers in both x and y directions. The 1 mil clear area at the center of this cell is not drawn to scale.

2. Diode mask 2 consists of a very small array as shown in the sketch. This geometry is also to be step and repeated on 0.260" centers in both x and y directions. The center lines of this drawing align with the center lines of mask 1. All dimensions of mask 2 are in mils so that this art work consists of a very small area step and repeated on a relatively wide center.

3. Contact mask 3 is shown in two parts. Contact mask 3a illustrates the large dimensions; contact mask 3b illustrates the

smaller dimensions located at the center and shown as a dashed inset on mask 3a. The finished mask consists of the combination of both these geometries, again to be step and repeated on 0.260" centers in both x and y dire directions. The center lines on all drawings should align with each other.

4. The Intraconnect Mask 4 has the geometry illustrated in sketch 4. This is a dark field mask in that the background is opaque. The art work is to be step and repeated on 0.260" centers in both x and y directions.

Masks 5 and 7 are those to be used with fabricating the diaphragm member of the structure.

1. Diaphragm Mask 5 represents a composite of the desired finished mask. It consists of a 5 x 5 array of 15 mil clear areas on 0.260" x 0.260" centers. Around the outside of this array is a 50 mil border with 5 mil grooves cut in the border so as to align with the edges of the 0.260" x 0.260" boundaries shown as reference lines. Note that the solid lines representing the boundaries of the cell will not appear on this mask. They are included for reference purposes only. This mask consists of a 5 x 5 array of clear circles on an opaque background surrounded by a border of rectangles and four-corner pieces as illustrated by the extra-heavy lines.

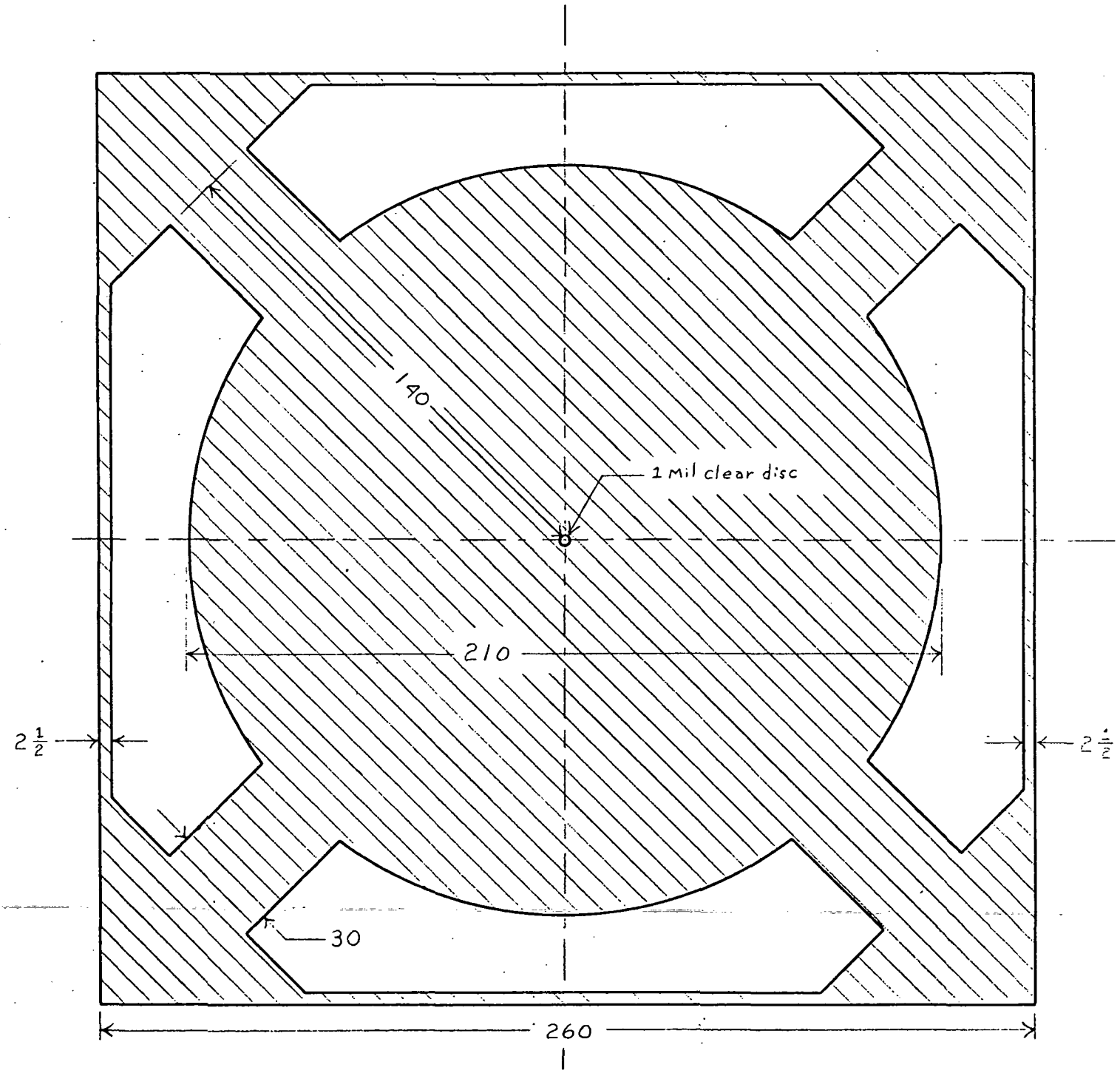
2. Diaphragm Mask 6 illustrates the geometry to be stepped and repeated on 0.260" x 0.260" centers.

3. Diaphragm Mask 7 illustrates the geometry to be step and repeated on 0.260" x 0.260" centers.

Masks 8 and 9 are for fabricating the regions of the cavity member of the structure. Each sketch illustrates the geometry for separate masks; this geometry is to be step and repeated on 0.260" x 0.260" centers for both masks 8 and 9.

Initial mask requirements for the RTI portion of the fabrication (Masks 5 thru 9) will be for three copies each. Masks 1-4 are to be used in fabricating the active element of the transducer. Those manufacturers making their own masks will determine their own requirements for this fabrication. For those manufactureres desiring RTI to supply the masks, a statement of the quantity of masks to be supplied is nec necessary.

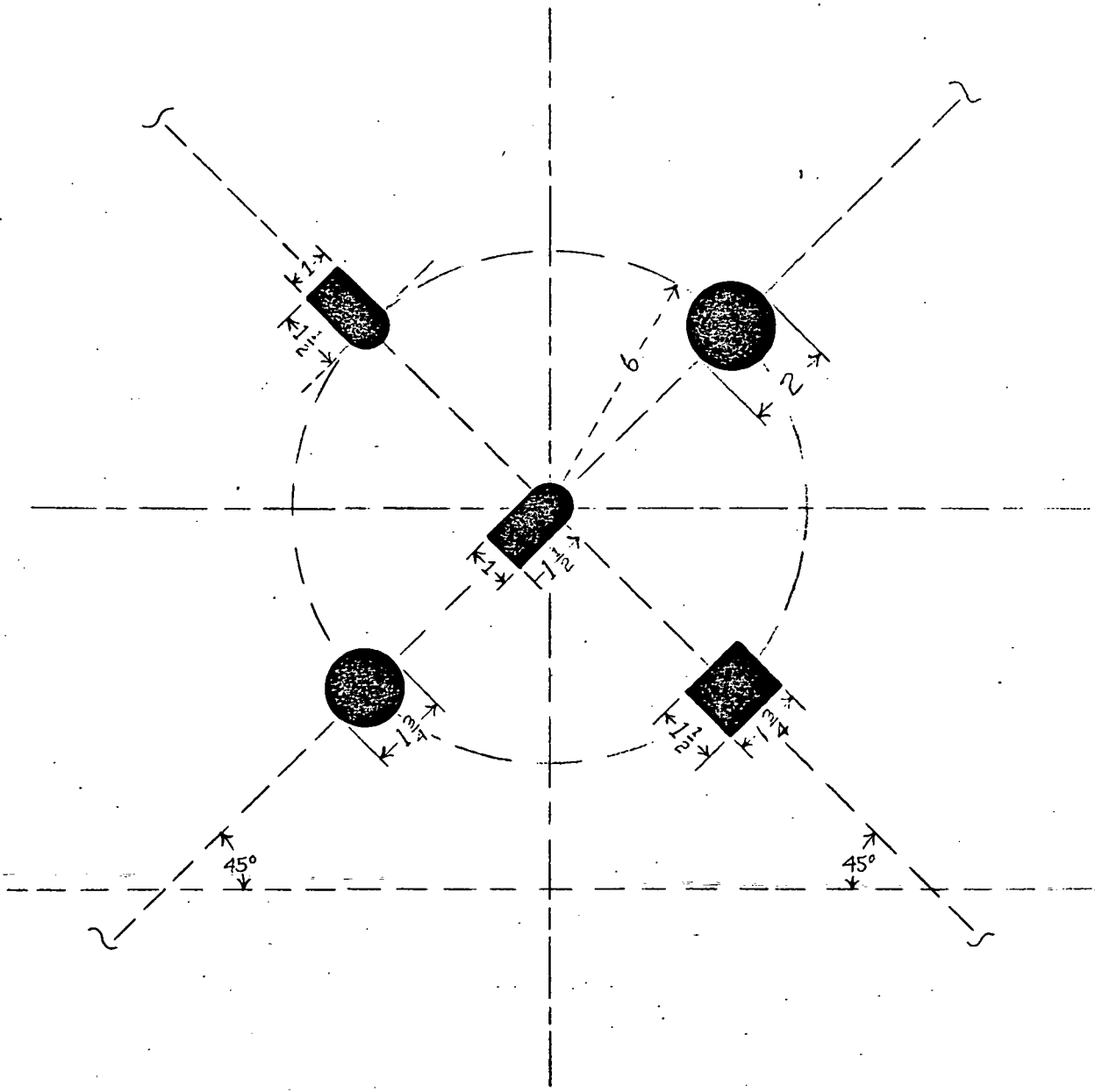
Mesa Mask #1



Note: All dimensions in mils
All shaded areas to be dark

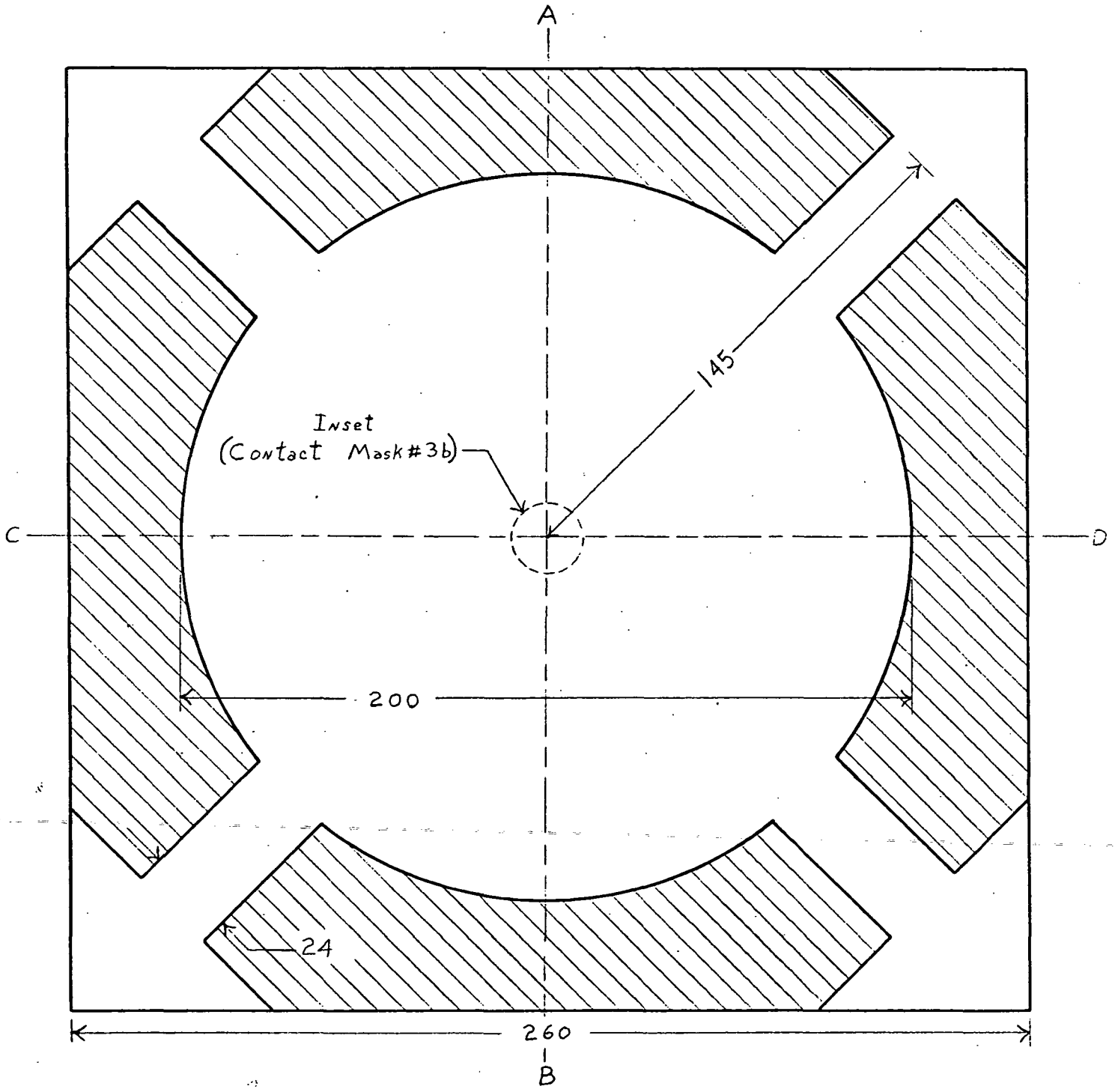
Scale: ¼"= 10 Mils

Diode Mask #2
Clear Field



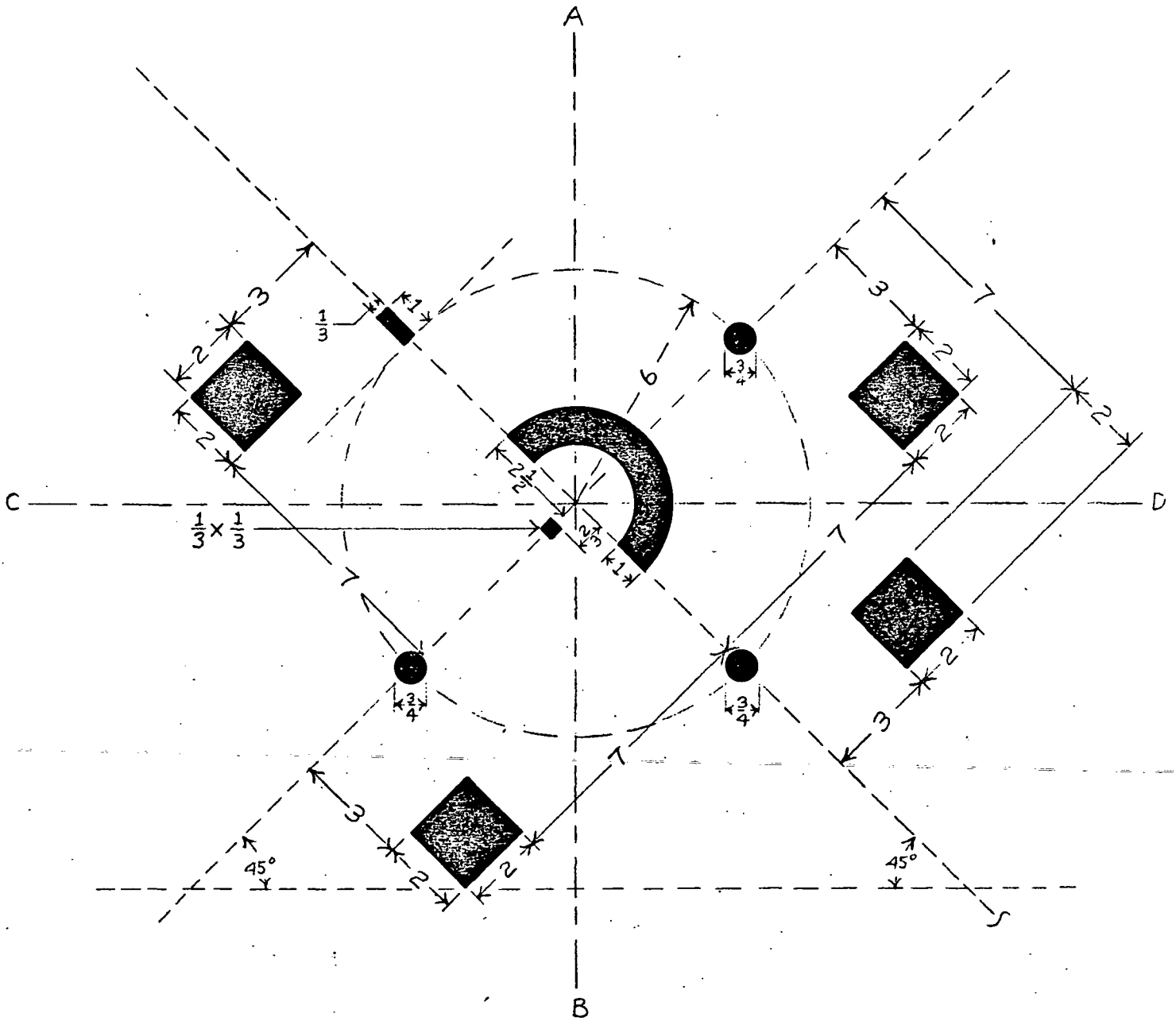
Scale: ¼" = 1 mil

Contact Mask #3a



Scale: ¼" = 10 mils.

Contact Mask #3b
Clear Field

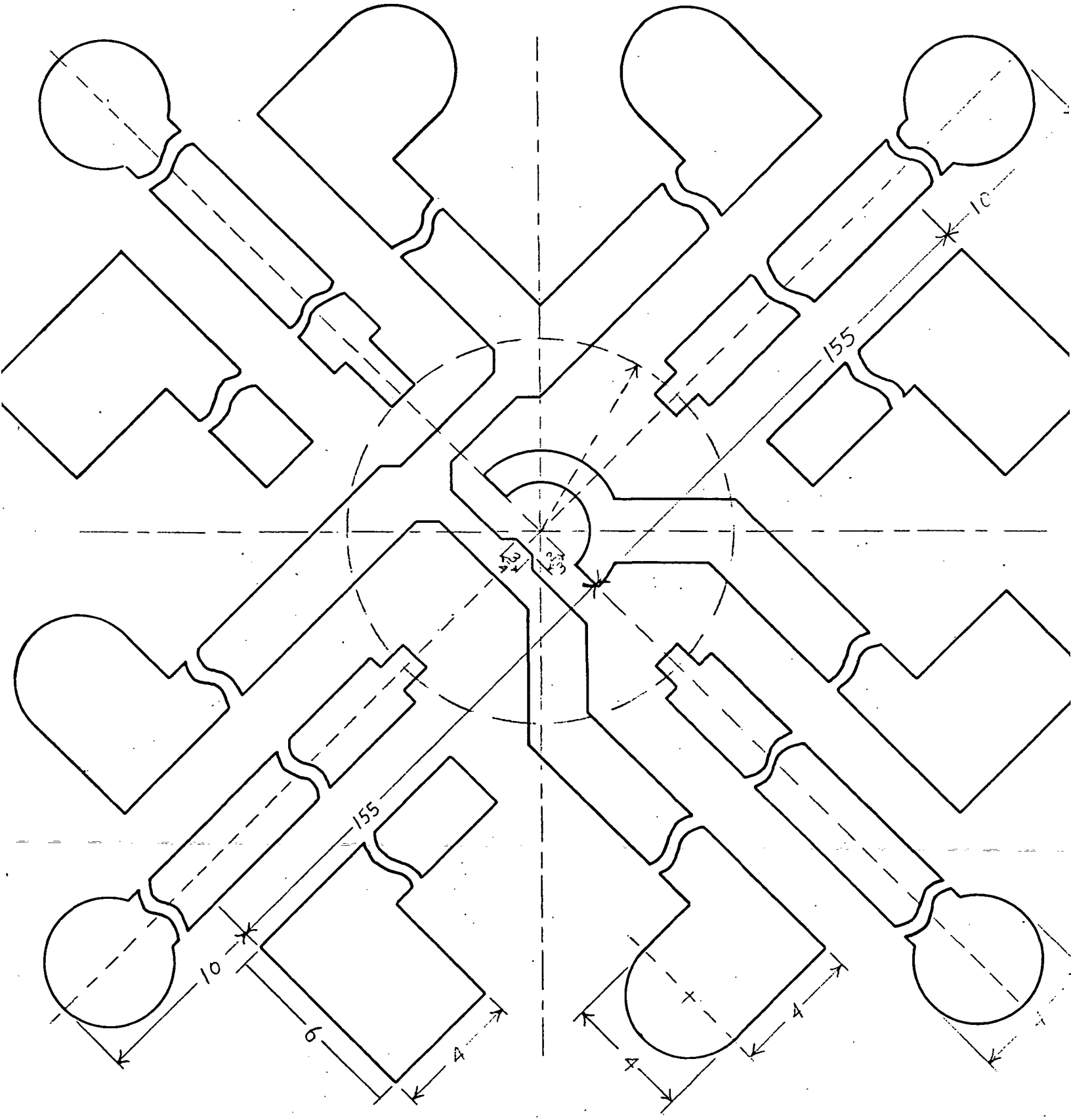


Scale: ¼" = 1 mil

Scale: $\frac{1}{4}" = 1$ mil

Intraconnect Mask #4

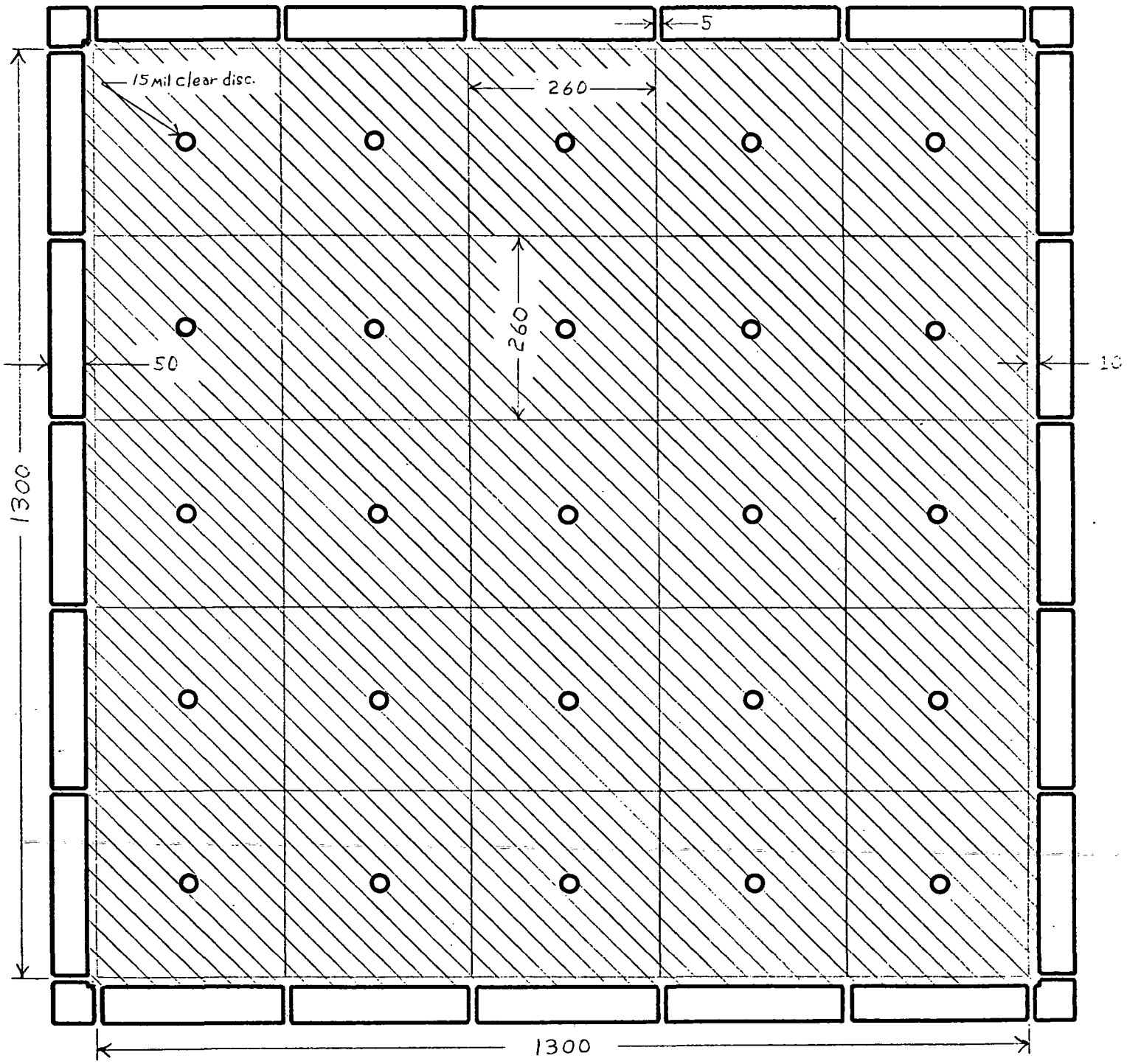
Dark Field



Note: All stripes are either 1 or 2 mils wide

Scale: ¼" = 1 mil

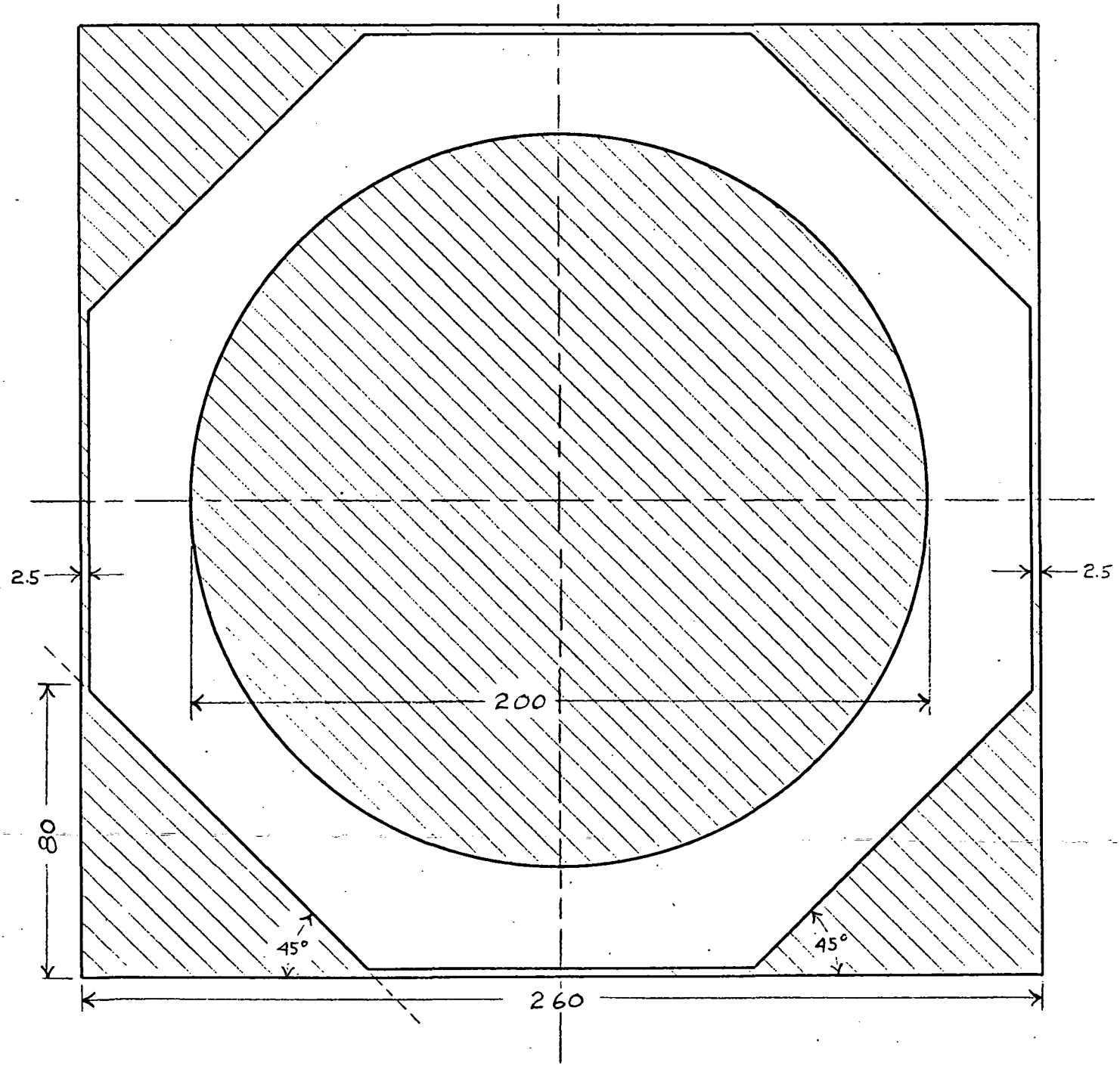
Diaphragm Mask #5



Extra heavy lines are only lines on mask; other solid lines are reference lines, showing position of step and repeat cell (.26 × .26). Shaded area is opaque.

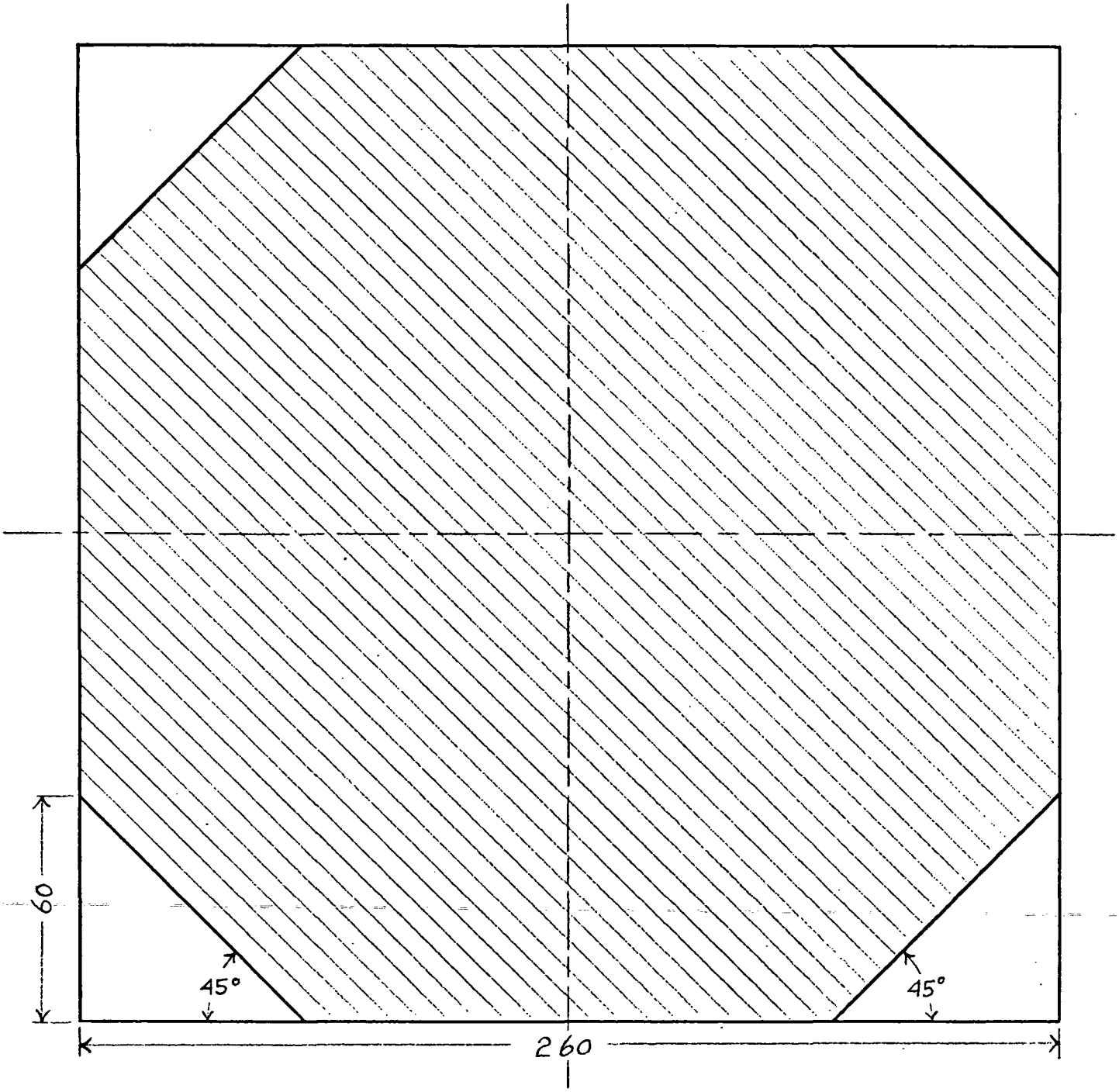
Scale: ¼"=50 Mils

Diaphragm Mask #6



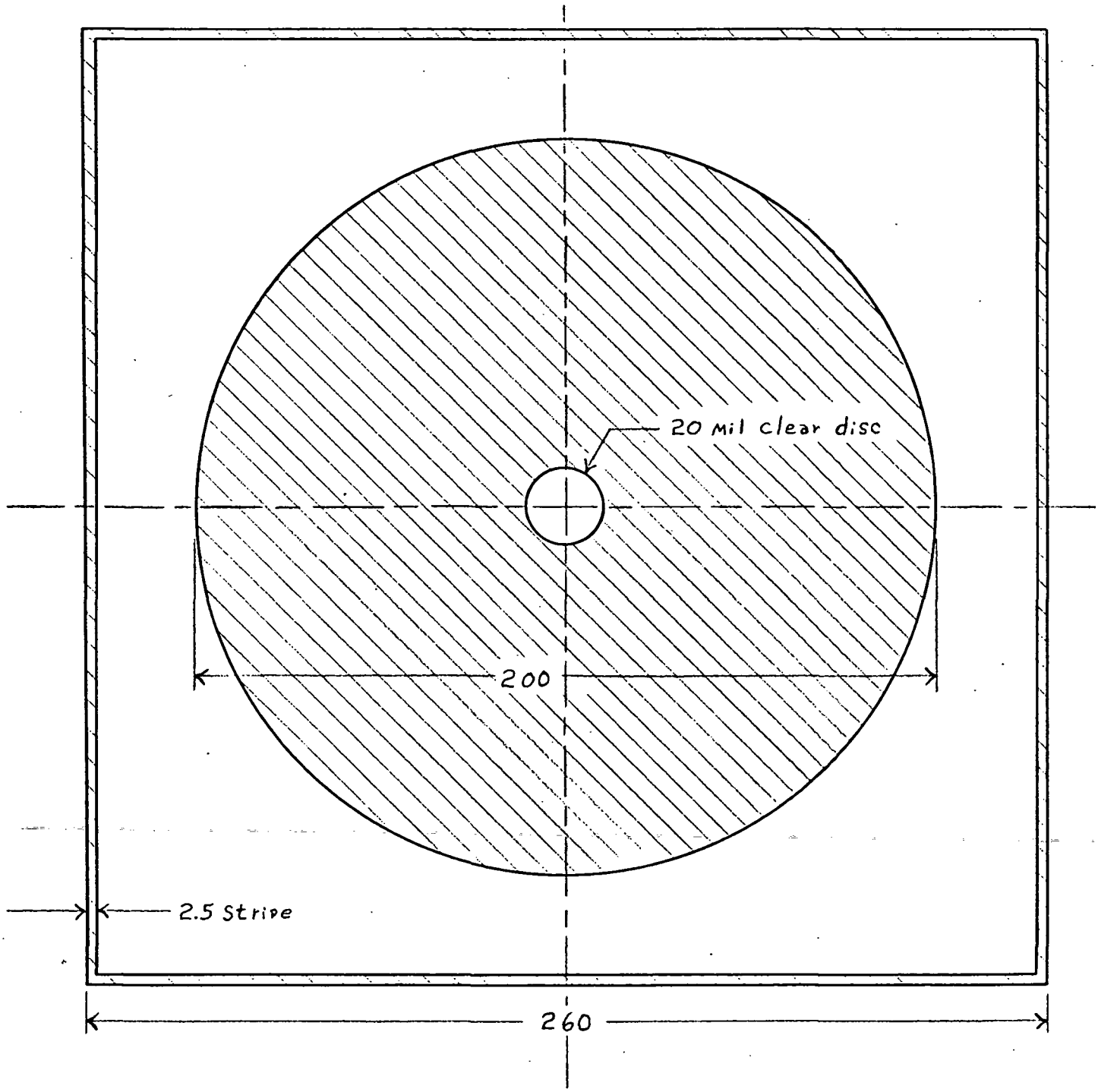
Scale: ¼" = 10 mils

Diaphragm Mask #7



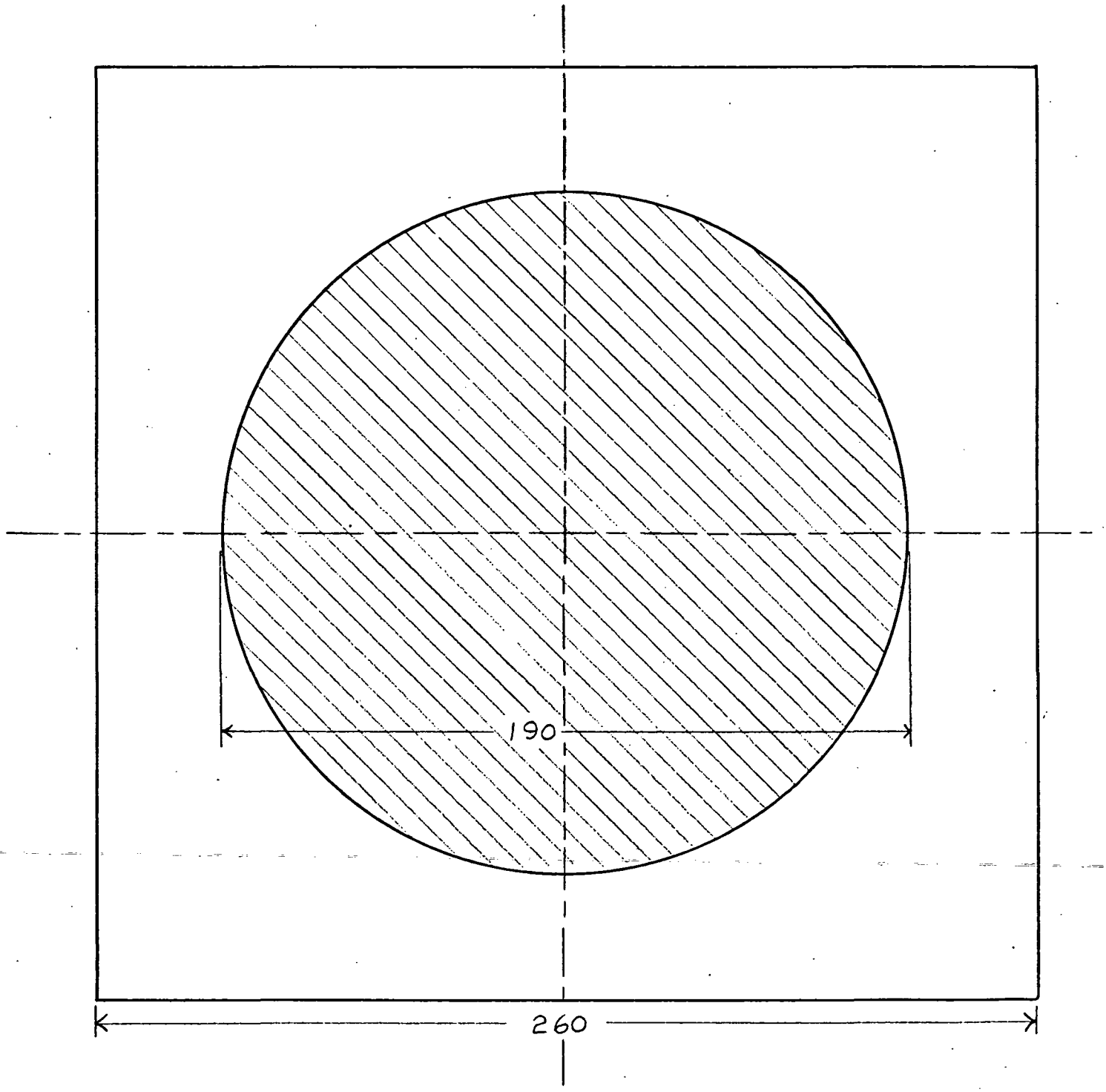
Scale: ¼" = 10 mils

Cavity Mask #8



Scale: ¼" = 10 mils

Cavity Mask #9



Scale: ¼" = 10 mils

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